

Commercial DT  
Project name: vWolverine  
Project code: 3PD089010001  
PCB Size : 203mm X 244mm  
PCB Number : 16528-1 (6 Layer)

PAGE	TITLE
01	COVER PAGE
02	BLOCK DIAGRAM
03	AM4 PCIE I/F
04	AM4 MEM DDR4
05	AM4 DISPLAY/MISC
06	AM4 ACPI/AZ/SD/I2C/GPIO
07	AM4 CLK/LPC/SPI/USB
08	AM4 POWER
09	AM4 GND (VSS)
10	AM4 Power CAP
11	PROMONTORY Power Cap
12	DDR4 DIMM4(A0)
13	DDR4 DIMM3(B0)
14	DDR4 DIMM2(A1)
15	DDR4 DIMM1(B1)
16	STRAP PINS
17	PROMONTORY PCIE/SATA
18	PROMONTORY GPIO
19	PROMONTORY USB/CLOCK
20	PROMONTORY POWER
21	(Reserved)
22	(Reserved)
23	(Reserved)
24	SIO ITE8739
25	Flash&RTC
26	Thermal&FAN
27	Audio Codec ALC662-VD
28	(Reserved)
29	Audio IO Front
30	Audio IO Rear
31	LAN RTL8111EPV
32	RJ45&Transformer
33	(Reserved)
34	(Reserved)
35	(Reserved)
36	USB20 REAR PORT
37	USB20 FRONT HEADER
38	USB30 REAR PORT
39	USB30 FRONT HEADER
40	Power Sequence Ctrl
41	Dual Power
42	USB SW Power
43	ATX(BATT Conn)
44	Power Sequence(DDR4)
45	DCDC-3D3V&5V
46	ISL6377 CPUCORE(1/3)
47	ISL6377 CPUCORE(2/3)
48	ISL6377 CPUCORE(3/3)
49	LDO APL1085 5V/3D3V
50	APL5337K VCCGFXOUT 0D775V
51	DC2DC VDDQ 1D2V RT8231A
52	DC2DC 1D05V RT8237
53	DCDC VDDIO 1D5V APL5930
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PAGE	TITLE
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56	(Reserved)
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58	CRT
59	(Reserved)
60	HDD/ODD
61	M.2 WLAN Key E
62	M.2 SSD Key M
63	(Reserved)
64	LED Board/Power Button
65	Others
66	(Reserved)
67	COM PORT
68	Debug port
69	LPT
70	(Reserved)
71	(Reserved)
72	(Reserved)
73	(Reserved)
74	(Reserved)
75	(Reserved)
76	(Reserved)
77	(Reserved)
78	(Reserved)
79	(Reserved)
80	(Reserved)
81	(Reserved)
82	(Reserved)
83	(Reserved)
84	(Reserved)
85	(Reserved)
86	(Reserved)
87	(Reserved)
88	(Reserved)
89	(Reserved)
90	(Reserved)
91	TPM
92	PS2
93	Express Card PCIeX16
94	Smart Card PCIeX1
95	(Reserved)
96	EMI
97	(Reserved)
98	(Reserved)
99	HDT
100	Table of Content
101	GPIO table
102	Power Sequence
103	Power Block Diagram
104	Power seq. Block Diagram
105	CLOCK MAP
106	RESET Flow CHART
107	Change History

BOM Configuration

Un-mount:(R\_)  
HDT:(HDT\_)  
TPM header: (H\_)  
LAN RTL8111EPV: (B\_)  
HDMI(D\_)  
LAN RTL8111E: (E\_)  
4DIMM SKU(M\_)  
CORETYPE(C\_)  
BR ONLY(BR\_)

PCH1 : PROM2 (KI.B3502.001)

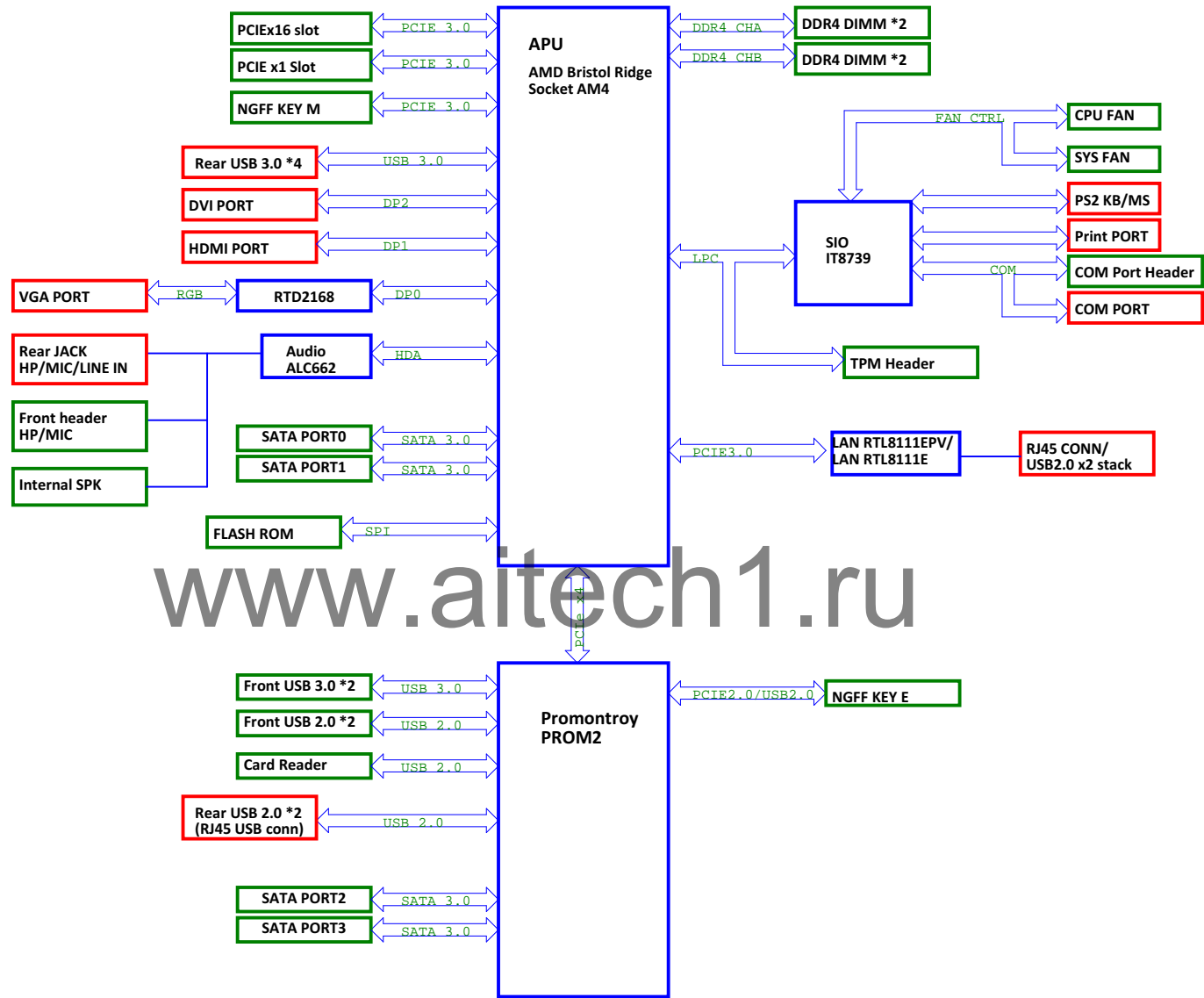
Key IC	
CPU1	AMD AM4 Bristol Ridge 65W
PCH1	PROM2 B350
SIO1	ITE ECIO IT8739E
U2701	Realtek ALC662-VD
U3101	Realtek RTL8111EPV/RTL8111E
U5801	Realtek converter RTD2166

Power sates		G3	EUP	S5	S4	S3	S0
+12V	12V_S0						0
	12V_CPU_S0						0
-12V	-12V_S0						0
	5V_LPS		0	0	0	0	0
5V	5V_USB_R			0	0	0	0
	5V_USB_F						
	5V_USB30P1						
	5V_USB30P2						
	5V_USB30P3						
	5V_USB30P4						
	5V_USB20P1						
	5V_USB20_RJUSB1						
	5V_USB20_RJUSB2						
	5V_USB20H1			0	0	0	0
	5V_USB20H2						
	5V_USB30H1						
3.3V	5V_USB30H2						
	5V_S0						0
	5V_DVI						
	5V_HDMICON_S0						
3.0V	3D3V_LPS		0	0	0	0	0
	V_3P3_LAN						
	3D3V_S5			0	0	0	0
2.5V	3D3V_S0						0
	3V_VBAT1_G3	0	0	0	0	0	0
1.5V	2D5V_S5_MEMVFP				0	0	0
	A_VBAT	0	0	0	0	0	0
1.2V	1D5V_S5			0	0	0	0
	V_1P2_LAN						0
	1D05V_S5_PROM			0	0	0	0
	1D05V_S5						
1.05V	1D05V_S0_PCH						0
	1D05V_S0						
	1D2V_VDDIO_MEM					0	0
DIMM	3D3V_S5_PCH			0	0	0	0
	3D3V_S0_PCH						
PCH	2D5V_S0_PCH						0
	1D05V_S0_PROM						
CPU	1D5V_VDDBT_RTC	0	0	0	0	0	0
	VDDCR_SOC_S5			0	0	0	0
	1V_VDDCR_CPU						
	3D3V_S0_SOC						0
	1V_VDDCR_SOC						

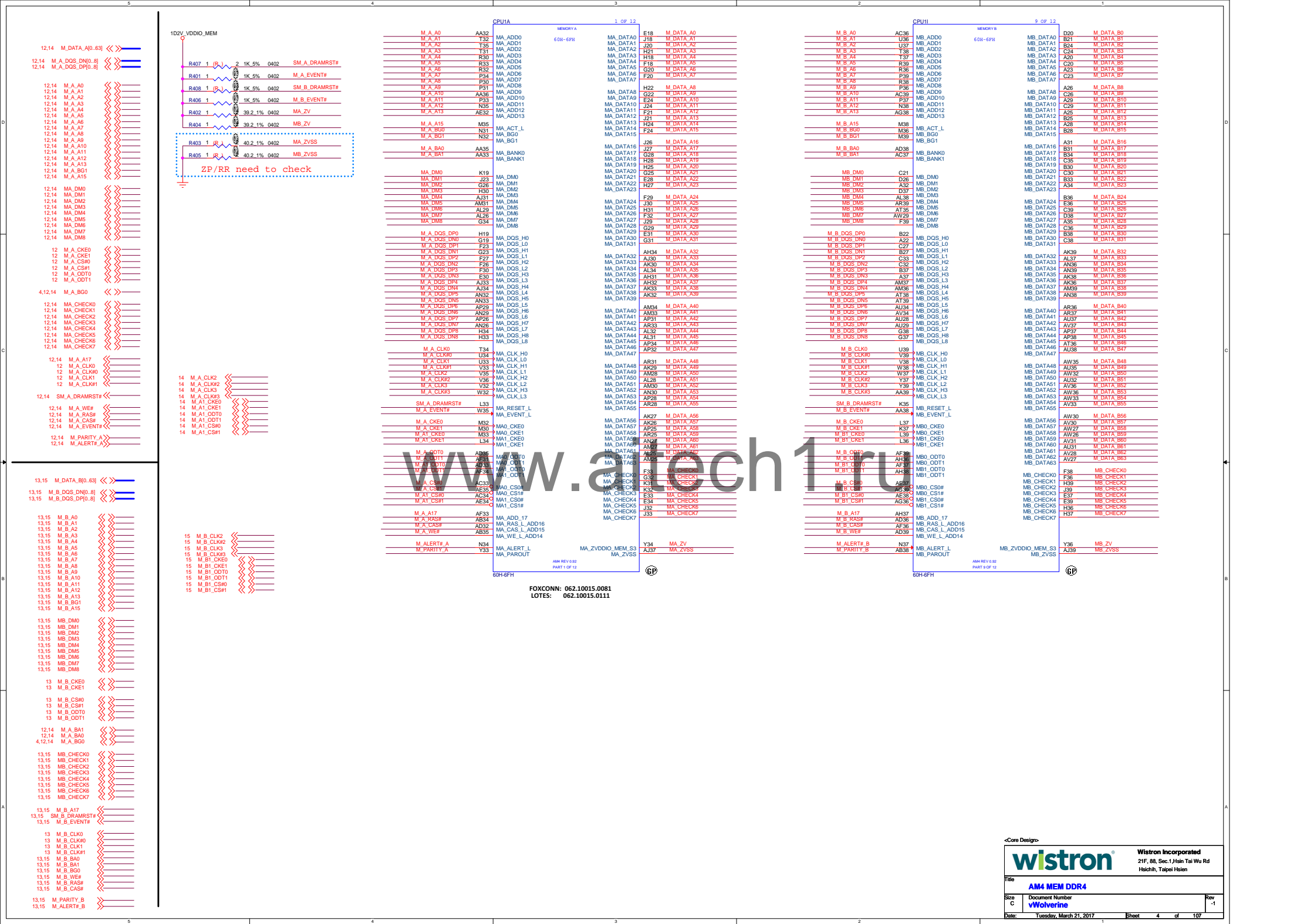
PROJECT NAME: vWolverine  
MB VERSION: -1

PCB BOARD SIZE: DTX

Internal Slot/Header  
Front/Rear IO  
Chipset

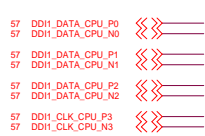








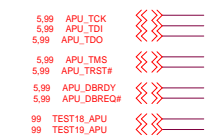
## DDI1 TO HDMI1



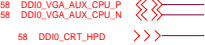
## DDI0 TO DP to VGA



## HDT



## USE for HDMI



## USE for VGA



## SVID

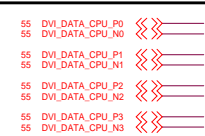


## 24 AMDTSI\_DATA\_CPU &lt;&lt;&gt;&gt;

## 24 AMDTSI\_CLK\_CPU &lt;&lt;&gt;&gt;

## 46 VR\_HOT#\_SIO &lt;&lt;&gt;&gt;

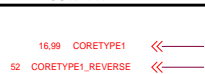
## DDI2 TO DVI



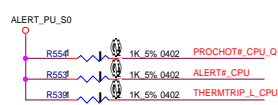
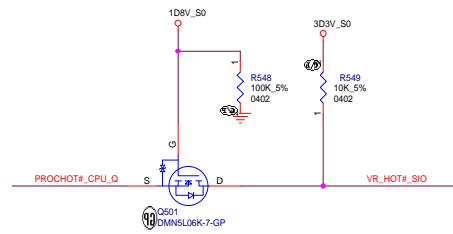
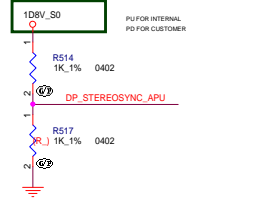
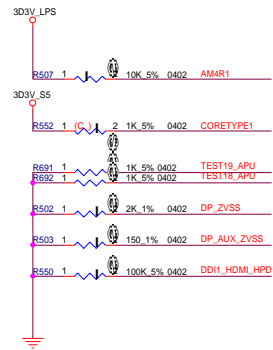
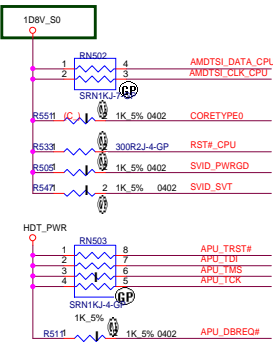
## USE for DVI



## CORETYPE



## 24 PROCHOT#\_CPU\_Q &lt;&lt;&gt;&gt;



## DDI2 TO DVI

## DDI1 TO HDMI1

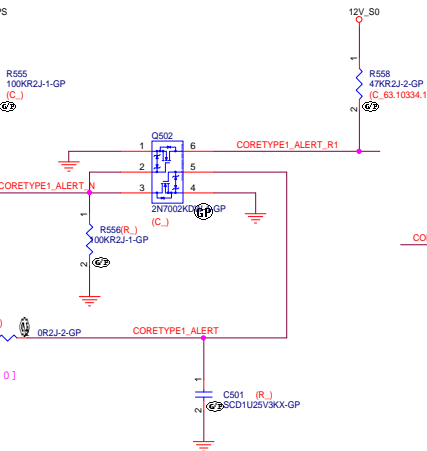
## DDI0 TO DP to VGA



## HDT



## CORETYPE DEFINITION[1:0]





38 USB\_CPU\_PN0 <<>>  
38 USB\_CPU\_PP0 <<>>  
38 USB\_CPU\_PN1 <<>>  
38 USB\_CPU\_PP1 <<>>

38 USB\_CPU\_PN2 <<>>  
38 USB\_CPU\_PP2 <<>>  
38 USB\_CPU\_PN3 <<>>  
38 USB\_CPU\_PP3 <<>>

38 USB30\_TX\_CPU\_P0 <<====  
38 USB30\_TX\_CPU\_N0 <<====

38 USB30\_RX\_CPU\_P0 >>====  
38 USB30\_RX\_CPU\_N0 >>====

```

38 USB30_TX_CPU_N1 <<=====
38 USB30_TX_CPU_P1 <<=====

38 USB30_RX_CPU_N1 >>=====
38 USB30_RX_CPU_P1 >>=====

```

```

38 USB30_TX_CPU_P2  <==
38 USB30_TX_CPU_N2  <==

38 USB30_RX_CPU_P2  ==>
38 USB30_RX_CPU_N2  ==>

```

```

38 USB30_TX_CPU_N3 <==
38 USB30_TX_CPU_P3 <==

38 USB30_RX_CPU_N3 >==
38 USB30_RX_CPU_P3 >==

```

```

25 SPI_CS_CPU      <-----
25 SPI_CLK_CPU     <-----
25 SPI_SO_CPU      <-----
25 SPI_WP_CPU      <-----
25 SPI_HOLD_CPU    <-----
25 SPI_SI_CPU      <-----
25 SPI_WP_ROM_C2   <-----

```

19	GPP_CLK0P	⏏
19	GPP_CLK0N	⏏
93	PEG_CLK_CPU_P	⏏
93	PEG_CLK_CPU_N	⏏
94	PEG_CLK1_APU_P	⏏
94	PEG_CLK1_APU_N	⏏
62	PEG_CLK2_SSD_P	⏏
62	PEG_CLK2_SSD_N	⏏
31	PEG_CLK3_LAN_P	⏏
31	PEG_CLK3_LAN_N	⏏

01 LPC\_AD\_SIO\_P0 <<>> \_\_\_\_\_

01 LPC\_AD\_SIO\_P1 <<>> \_\_\_\_\_

01 LPC\_AD\_SIO\_P2 <<>> \_\_\_\_\_

01 LPC\_AD\_SIO\_P3 <<>> \_\_\_\_\_

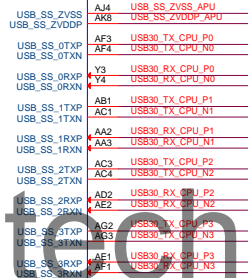
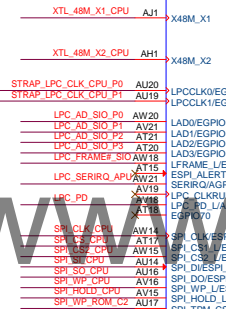
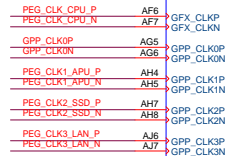
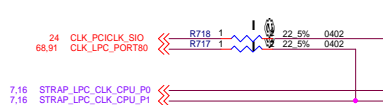
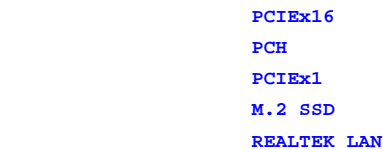
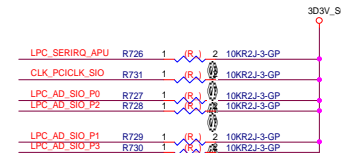
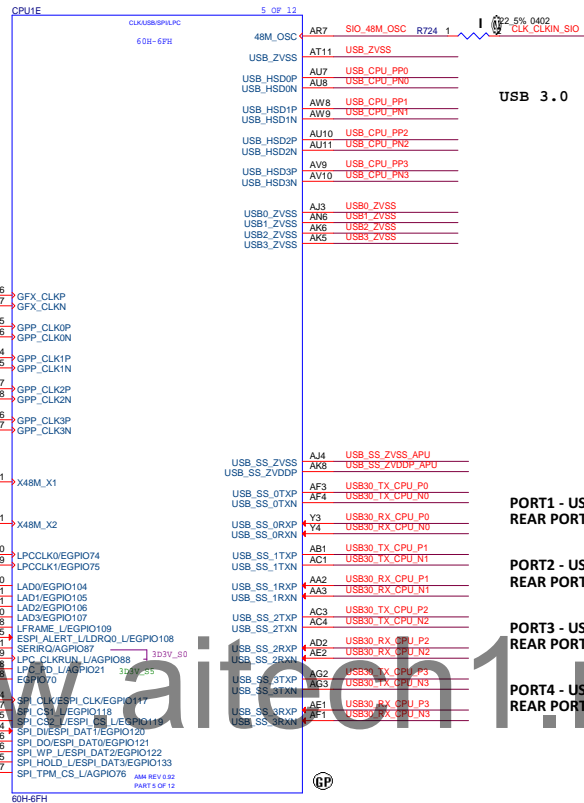
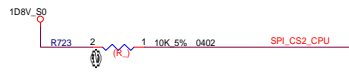
4,68,91 LPC\_FRAME#\_SIO <<>> \_\_\_\_\_

7.16 STRAP\_LPC\_CLK\_CPU\_P0 

7.16 STRAP\_LPC\_CLK\_CPU\_P1 

24,91 LPC\_SERIRQ\_APU >> \_\_\_\_\_

24 CLK\_CLKIN\_SIO >> \_\_\_\_\_

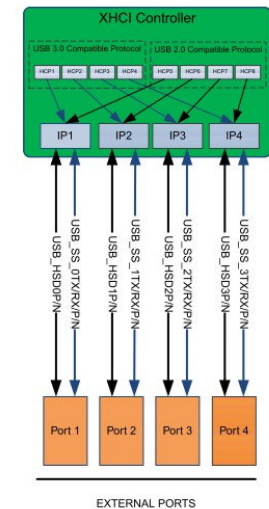
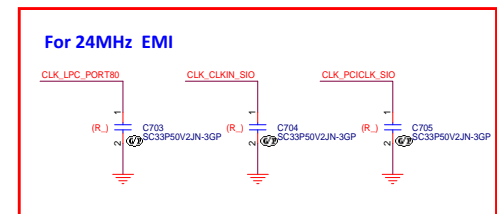


PORT1 - USB30  
REAR PORT

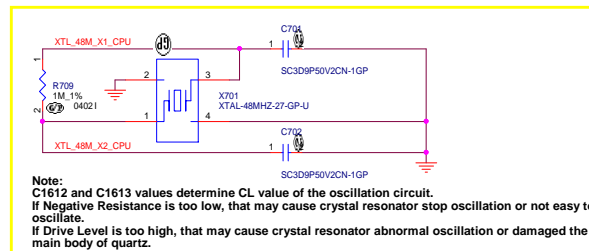
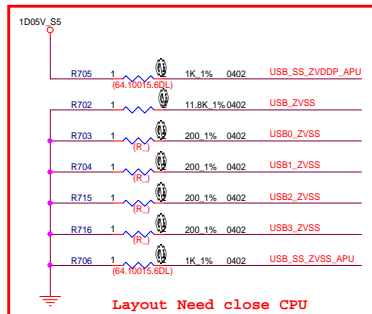
PORT2 - USB30  
REAR PORT

PORT3 - USB30  
REAR PORT

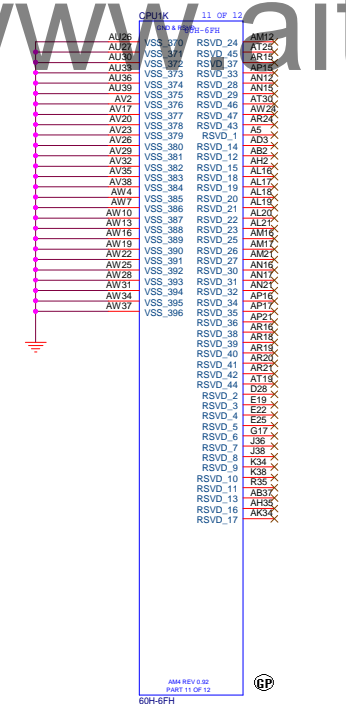
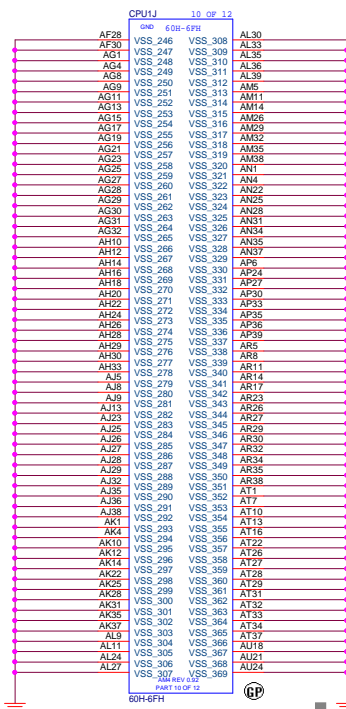
PORT4 - USB30  
REAR PORT



- Type 0 and Type 2 AM4 processors: Ports 1-4 are USB 3.1 Gen 1 capable
- Type 3 AM4 processor: Port 1 is USB 3.1 Gen 1 capable. Ports 2-4 are USB 3.1 Gen 2 capable

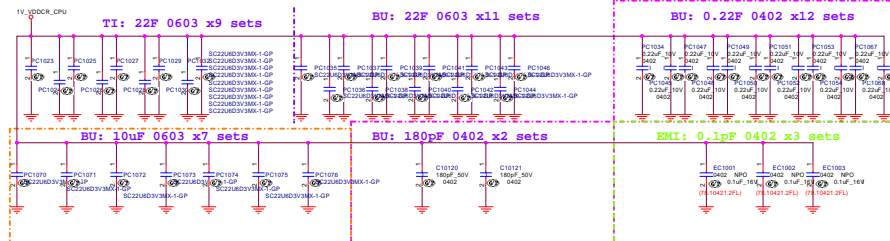






Microcontroller pinout diagram for the ATmega64H. The diagram shows a top view of the chip with pins numbered 1 to 40. Pin 1 is labeled 'GND'. Pin 2 is labeled 'VCC'. Pin 3 is labeled 'VCC'. Pin 4 is labeled 'VCC'. Pin 5 is labeled 'VCC'. Pin 6 is labeled 'VCC'. Pin 7 is labeled 'VCC'. Pin 8 is labeled 'VCC'. Pin 9 is labeled 'VCC'. Pin 10 is labeled 'VCC'. Pin 11 is labeled 'VCC'. Pin 12 is labeled 'VCC'. Pin 13 is labeled 'VCC'. Pin 14 is labeled 'VCC'. Pin 15 is labeled 'VCC'. Pin 16 is labeled 'VCC'. Pin 17 is labeled 'VCC'. Pin 18 is labeled 'VCC'. Pin 19 is labeled 'VCC'. Pin 20 is labeled 'VCC'. Pin 21 is labeled 'VCC'. Pin 22 is labeled 'VCC'. Pin 23 is labeled 'VCC'. Pin 24 is labeled 'VCC'. Pin 25 is labeled 'VCC'. Pin 26 is labeled 'VCC'. Pin 27 is labeled 'VCC'. Pin 28 is labeled 'VCC'. Pin 29 is labeled 'VCC'. Pin 30 is labeled 'VCC'. Pin 31 is labeled 'VCC'. Pin 32 is labeled 'VCC'. Pin 33 is labeled 'VCC'. Pin 34 is labeled 'VCC'. Pin 35 is labeled 'VCC'. Pin 36 is labeled 'VCC'. Pin 37 is labeled 'VCC'. Pin 38 is labeled 'VCC'. Pin 39 is labeled 'VCC'. Pin 40 is labeled 'VCC'. The diagram also shows the internal structure of the chip, including the CPU, memory, and peripheral blocks.

## 1V\_VDDCR\_CPU



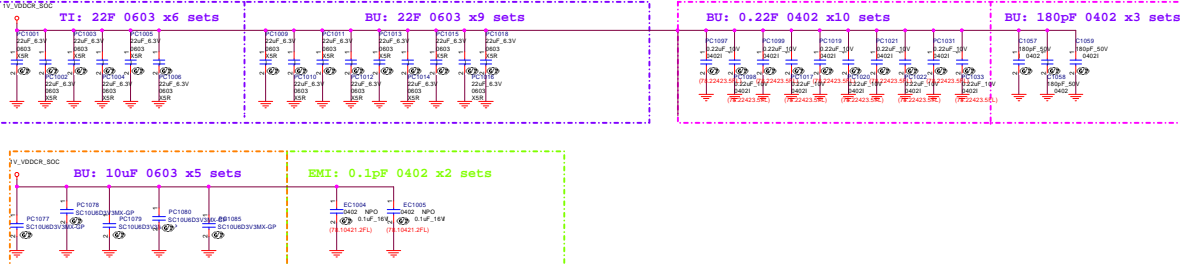
TI: The capacitors are placed on the top side (on the same side as the processor) of the board inside the processor socket cavity.

B: The capacitors are placed on the bottom side of the board.

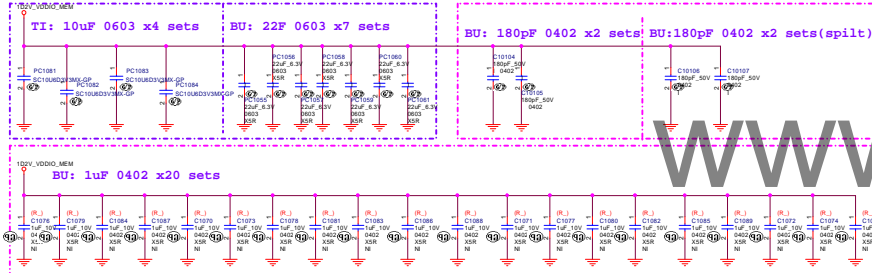
BU: The capacitors are placed on the bottom side of the board, under the processor socket, thereby allowing the shortest possible distance from the power pins.

S: indicates the capacitors are placed on the VDDIO\_MEM\_S3 plane split.

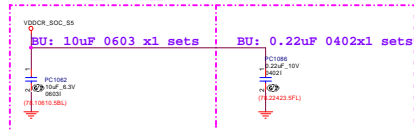
## 1V\_VDDCR\_SOC



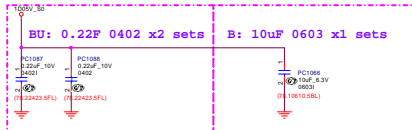
## 1D2V\_VDDIO\_MEM



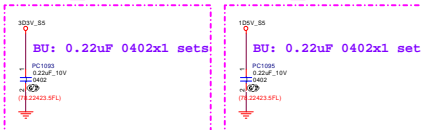
## VDDCR\_SOC\_S5



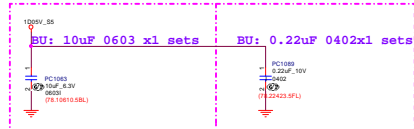
## 1D05V\_S0



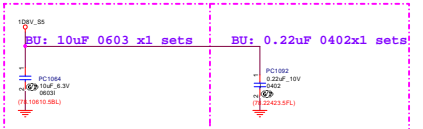
## 3D3V\_S5



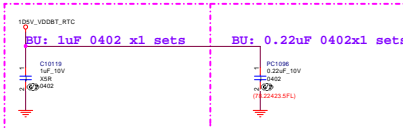
## 1D05V\_S5



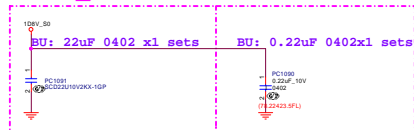
## 1D8V\_S5



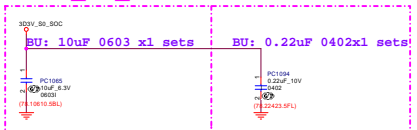
## 1D5V\_VDDBT\_RTC



## 1D8V\_S0



## 3D3V\_S0\_SOC



<Circ Design>

**wistron**

Wistron Incorporated  
21F, 8B, Sec 1, Hsin-Tsuei Rd  
Hsinchu, Taipei, Taiwan

AM4\_Power\_CAP

Doc Number

Version

Rev

Issue Date

Rev

100V50\_POM

22uF 0603 x5 sets

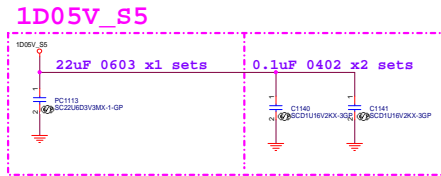
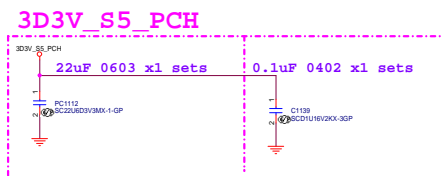
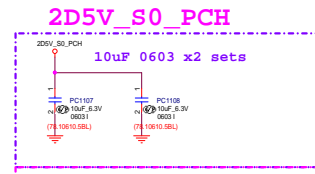
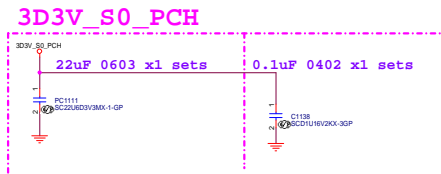
PC1101 SC22U0D3/3MX-1-GP

PC1102 SC22U0D3/3MX-1-GP

PC1103 SC22U0D3/3MX-1-GP

PC1104 SC22U0D3/3MX-1-GP

PC1105 SC22U0D3/3MX-1-GP

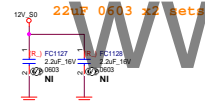
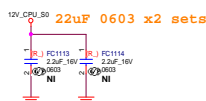
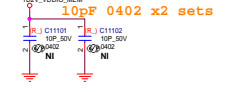
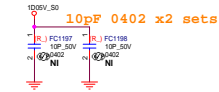
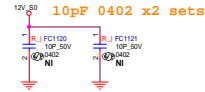
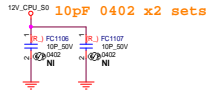


12V\_CPU\_50\_VCORE

10pF 0402 x2 sets

R<sub>J</sub> FC1104  
10P\_50V  
NI

R<sub>J</sub> FC1105  
10P\_50V  
NI

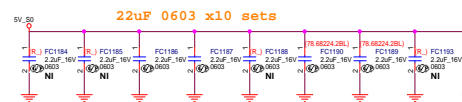
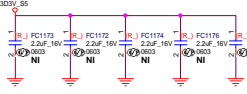
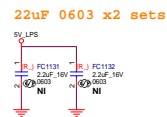
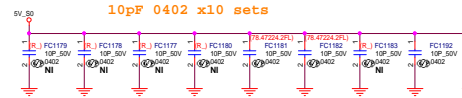
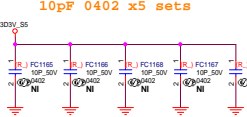


10pF 0402 x2 sets

5V LPS

FC1129 10P\_50V 0402 NI

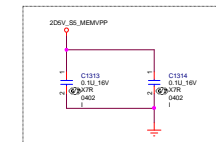
FC1130 10P\_50V 0402 NI





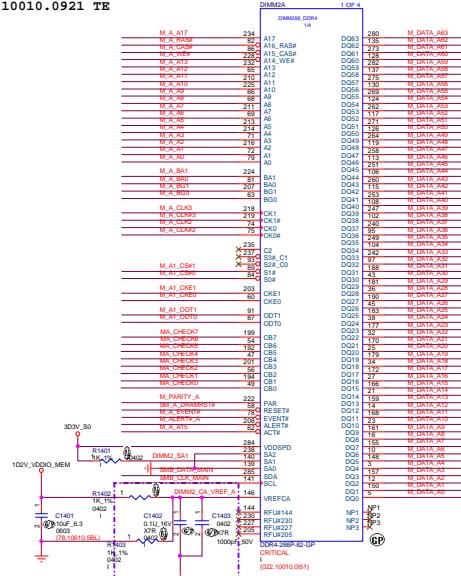
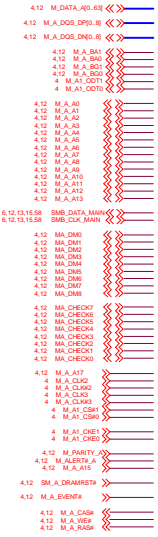


```
DDR4_288P(Housing:White/Ejector:White)
022.10010.0E21 TCONN
022.10010.0761 FOXCONN
022.10010.0931 TE
```

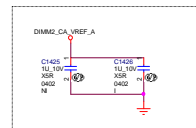


# CHANNEL A -- DIMM2(A1)

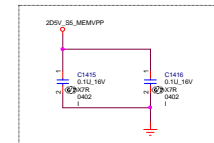
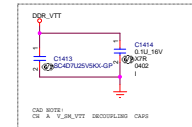
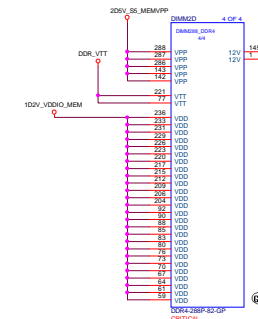
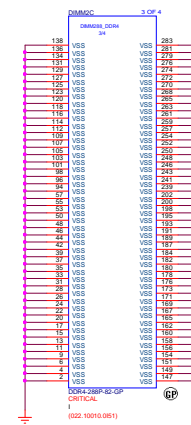
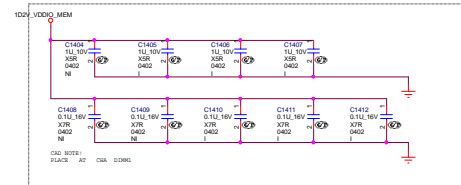
DDR4\_288P (Housing:Black/Ejector:White)  
022.10010.0E31 TCONN  
022.10010.0771 FOXCONN  
022.10010.0921 TE



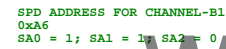
50724\_1\_02 / Page 173  
All the resistor and  
Capacitors are need to close  
at DIMM slot.



SPD ADDRESS FOR CHANNEL-A1  
0xA4  
SA0 = 0; SA1 = 1; SA2 = 0



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## FPU

7,24,68,91 LPC\_FRAME#\_SIO >>>  
6,61 SUS\_CLK\_CPU\_P1 >>>

7 STRAP\_LPC\_CLK\_CPU\_P0 <<<  
7 STRAP\_LPC\_CLK\_CPU\_P1 <<<

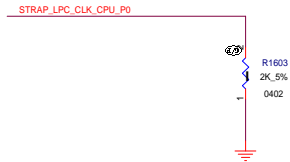
## PROM

18 PM\_PKG0 >>>  
18 PM\_PKG1 >>>  
18 PM\_SPI\_SCK >>>  
18 PM\_SPI\_SDI >>>  
18 PM\_SPI\_SDO >>>  
17 PM\_IFDET0 >>>  
17 PM\_IFDET1 >>>  
18 PM\_TESTEN >>>  
18 PM\_UART\_TX >>>  
18 PM\_DEBUG\_ENABLE >>>

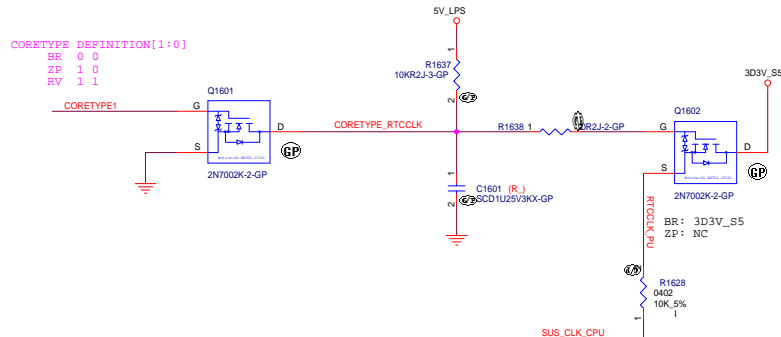
18 PM\_GPIO\_R4 >>>  
18 PM\_GPIO\_R5 >>>  
18 PM\_GPIO\_R6 >>>  
18 PM\_GPIO\_R7 >>>  
18 PM\_GPIO\_R8 >>>  
18 PM\_GPIO\_R9 >>>  
18 PM\_GPIO\_R10 >>>  
18 PM\_GPIO\_R11 >>>

5,99 CORETYPE1 <<<

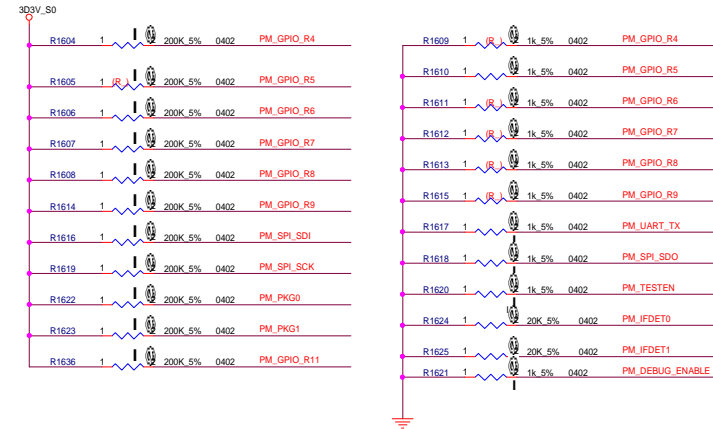
## AM4 FPU HW Strap



SIGNAL Name	Strap Name	Strap Type	Default Value	Bit Value	Description	Net name	Default Value
LFRAME_L	ROMTYPE	Strap II	1	0	LPC ROM	LPC_FRAME#_SIO	1
LPCLCK1	CLKGEN	Strap II	1	0	Reserved	STRAP_LPC_CLK_CPU_P1	1
LPCLCK0	BOOTFAILTIMER	Strap II	0	0	Configured for internal clock generator (Default)	STRAP_LPC_CLK_CPU_P0	0
RTCLCK	RTC Coin Battery	Strap I	1	0	Boot Fail Timer Disabled (Default) Boot Fail Timer Enabled RTC Coin Battery is not implemented RTC Coin Battery is not implemented	SUS_CLK_CPU	1
SYS_RESET_L	ShortReset	Strap I	1	0	Reserved	FP_RSTSW#	1
AGPIO3	Alternate Reset	Strap I	1	0	Normal powerup/ reset timing (Default) Traditional Reset logic 2 kΩ (± 5%) pull-down resistor to VSS	HOOD_SW_DET#	1
				1	Enhanced Reset logic (Default) for faster resume from S5 10kΩ (± 5%) pull-up resistor to VDD_33_S5 To ensure the strap can capture correct information, platform has to make sure AGPIO3 has valid voltage config value until 20 ms after RamRstB has risen to at least 3.0v. AGPIO3 can be used as a GPIO as long as the signal is not driven on during S5 to S0 (during Resume reset time)		



## PROM HW Strap



Signal Name	Function	Net name	Default Value
GPIO_R[4]	GPP clock source 1: From APUCLK 0: From EXT_Crystal	PM_GPIO_R4	1
GPIO_R[5]	USB SSC (Spread Spectrum Clock) 1: Disable (Default) 0: Enable	PM_GPIO_R5	1
GPIO_R[6]	SATA SSC (Spread Spectrum Clock) 1: Disable (Default) 0: Enable	PM_GPIO_R6	1
GPIO_R[7]	SATA Express SSC (Spread Spectrum Clock) 1: Disable (Default) 0: Enable	PM_GPIO_R7	1
GPIO_R[8]	GPP SSC (Spread Spectrum Clock) 1: Disable (Default) 0: Enable	PM_GPIO_R8	1
GPIO_R[9]	Whole Chip SSC (Spread Spectrum Clock) 1: Disable (Default) 0: Enable	PM_GPIO_R9	1
IFDET0	SATA Express port1 1: PCIe mode 0: SATA mode	PM_IFDET0	0
IFDET1	SATA Express port0 1: PCIe mode 0: SATA mode	PM_IFDET1	0
DEBUG_ENABLE	1: Function mode 0: Debug mode	PM_DEBUG_ENABLE	1
TESTEN	1: TEST mode Enable 0: TEST mode Disable	PM_TESTEN	0
UART_TX (GPP_G1_SET1) SPI_SDI (GPP_G1_SET0)	GPP Group1 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved	PM_UART_TX PM_SPI_SDI	0 1
SPI_SDO (GPP_G0_SET1) SPI_SCK (GPP_G0_SET0)	GPP Group0 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved	PM_SPI_SDO PM_SPI_SCK	0 1

<Core Design>

<b>wistron</b> Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsinchu	
File	STRAP_pins
Size	Document Number
C	vWolverine
Date	Tuesday, March 21, 2017
Sheet	16 of 107

## DMI

3 DMI\_RX\_CPU\_P0\_3] <<=====

3 DMI\_RX\_CPU\_N0\_3] <<=====

3 DMI\_TX\_CPU\_P0\_3] <<=====

3 DMI\_TX\_CPU\_N0\_3] <<=====

## PCIE

61 PCIE\_TX\_CON\_N0 <<=====

61 PCIE\_TX\_CON\_P0 <<=====

61 PCIE\_RX\_PCH\_N0 <<=====

61 PCIE\_RX\_PCH\_P0 <<=====

## SATA PORT

60 SATA\_TX\_PCH\_P0 <<=====

60 SATA\_TX\_PCH\_N0 <<=====

60 SATA\_RX\_PCH\_P0 <<=====

60 SATA\_RX\_PCH\_N0 <<=====

60 SATA\_TX\_PCH\_P1 <<=====

60 SATA\_TX\_PCH\_N1 <<=====

60 SATA\_RX\_PCH\_P1 <<=====

60 SATA\_RX\_PCH\_N1 <<=====

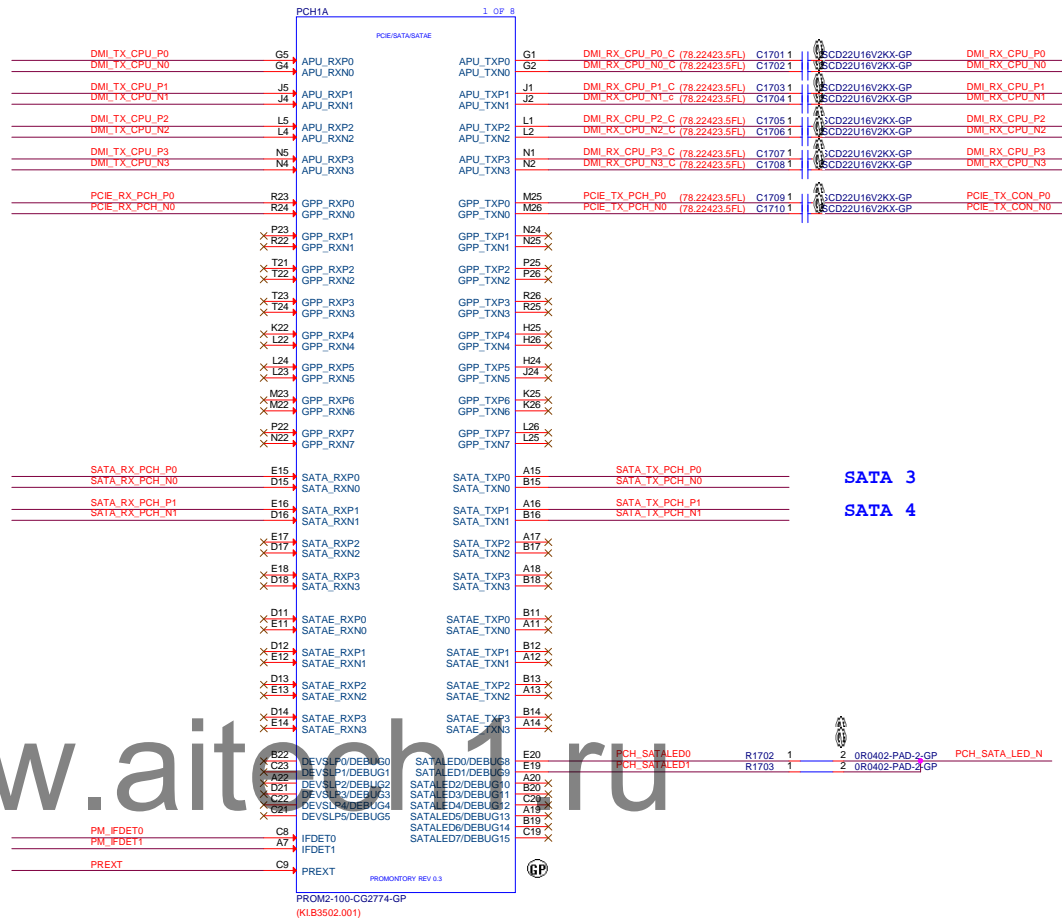
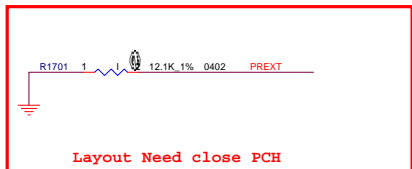
## SATA LED

64 PCH\_SATA\_LED\_N<<=====

## PROM

16 PM\_IFDET0 <<=====

16 PM\_IFDET1 <<=====



# STRAP

16 PM\_PKG0 <<  
16 PM\_PKG1 <<  
16,18 PM\_DEBUG\_ENABLE <<  
16 PM\_SPL\_SCK <<  
16 PM\_SPL\_SDI <<  
16 PM\_SPL\_SDO <<  
16,17 PM\_IFDET0 <<  
16,17 PM\_IFDET1 <<  
16 PM\_TESTEN <<  
16 PM\_UART\_TX <<  
16 PM\_GPIO\_R4 <<  
16 PM\_GPIO\_R5 <<  
16 PM\_GPIO\_R6 <<  
16 PM\_GPIO\_R7 <<  
16 PM\_GPIO\_R8 <<  
16 PM\_GPIO\_R9 <<  
16 PM\_GPIO\_R11 <<  
16,18 PM\_DEBUG\_ENABLE <<

# RST

6,93 PM\_GPIO0\_X16\_PRSTNT >>  
61 PCHRST\_WLAN >>  
31 PCHRST\_LAN >>

# SIO

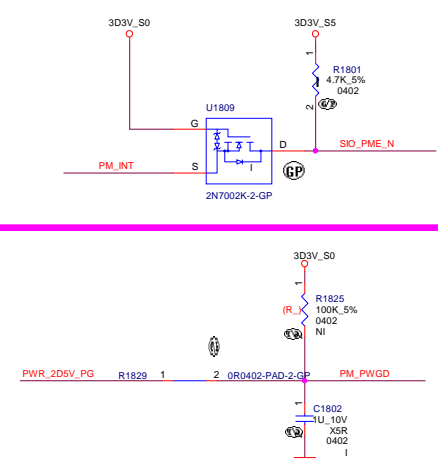
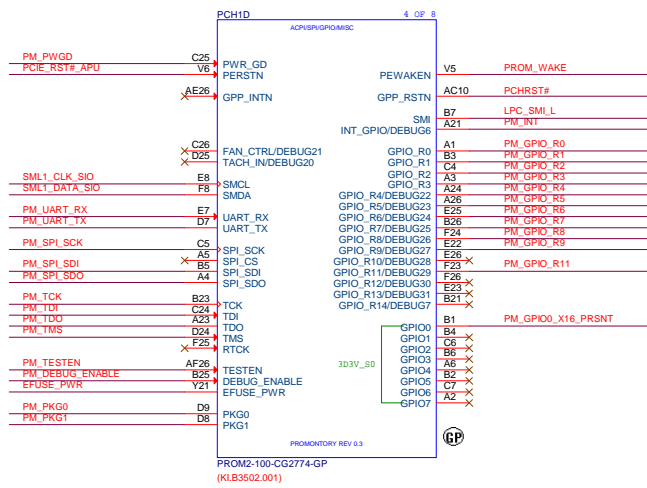
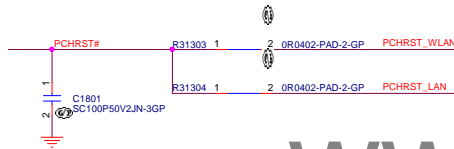
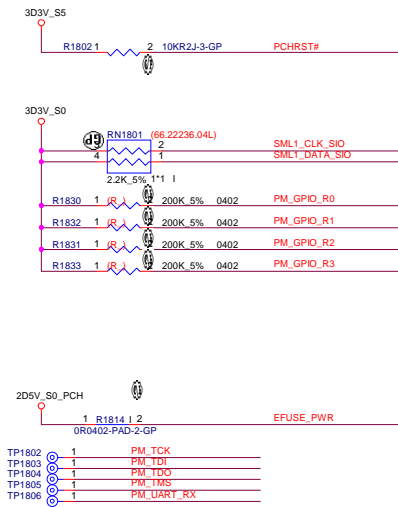
6,24 SIO\_PME\_N <<

# OTHER

46 PM\_PWGD <<  
44 PWR\_2D5V\_PG <<  
6 LPC\_SML\_L <<

Output To APU  
6 PROM\_WAKE <<

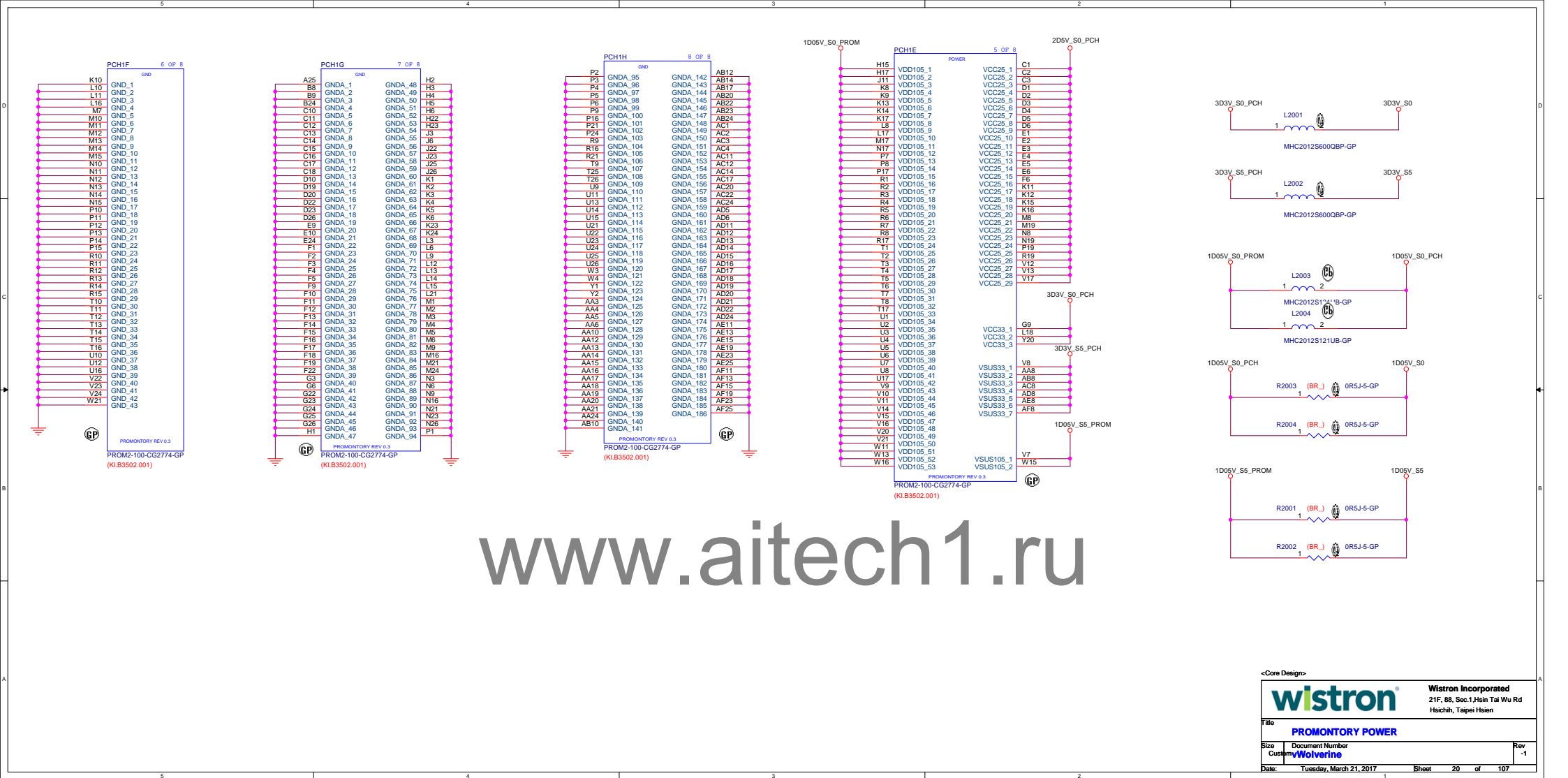
Output To APU  
6 PCIE\_RST#\_APU >>



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<Core Design>

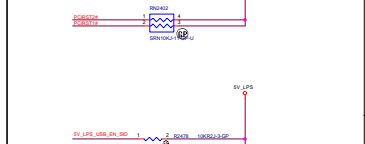
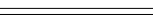
**wistron** Wistron Incorporated  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title		
PROMONTORY POWER		
Size	Document Number	Rev
Customer	Wolverine	-1
Date:	Tuesday, March 21, 2017	Sheet 20 of 107

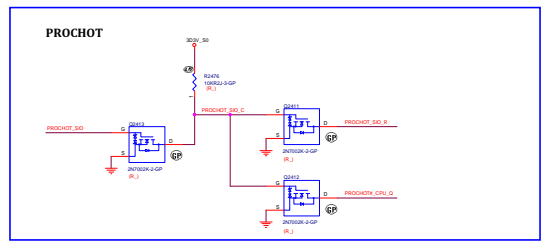
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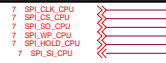


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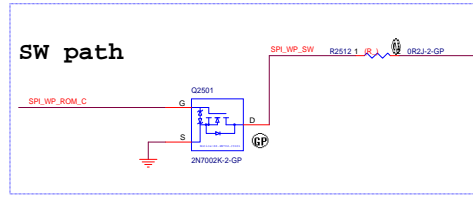
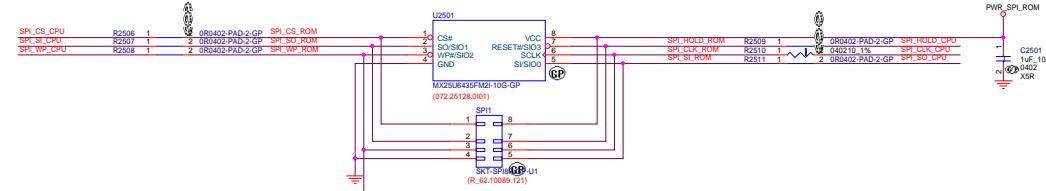
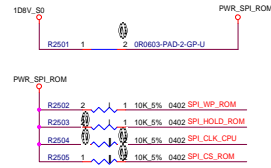
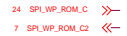


# SPI ROM

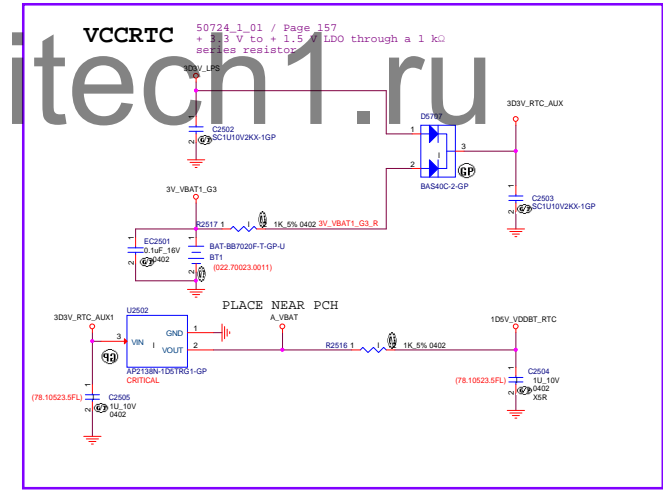
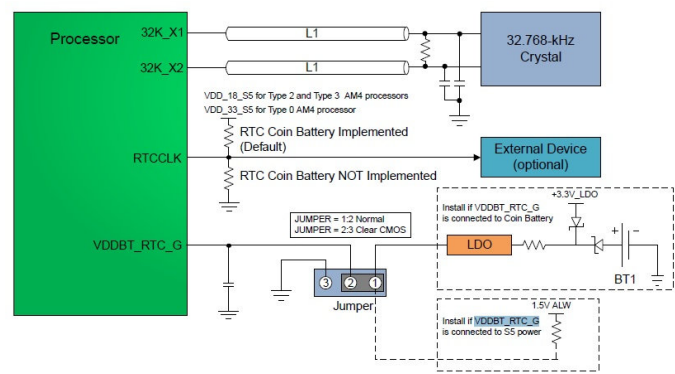
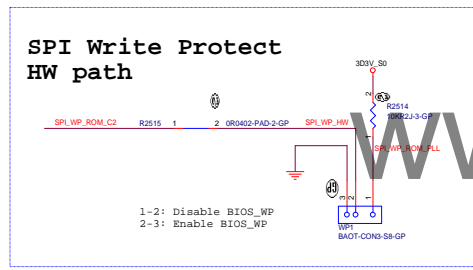
## CPU



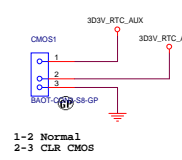
## WP



2015/03/03-1A Vita  
Add SW/WW path for BIOS WP



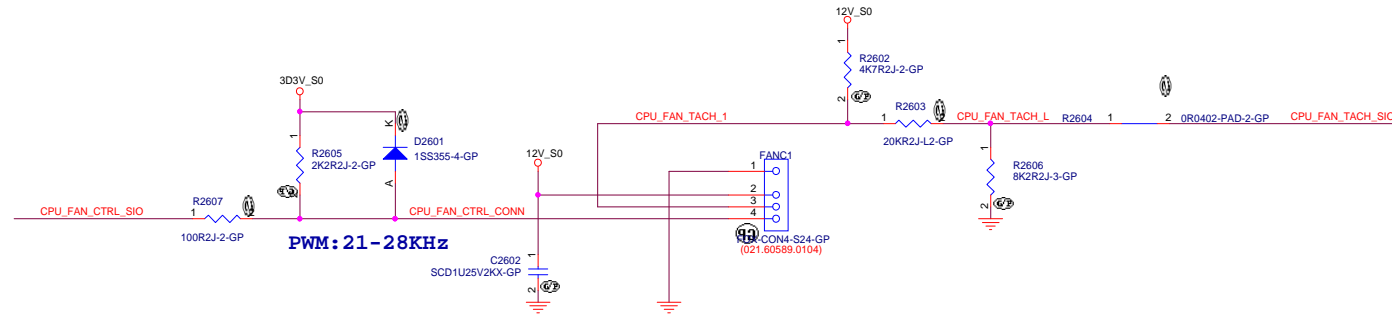
## CMOS CLR JUMPER





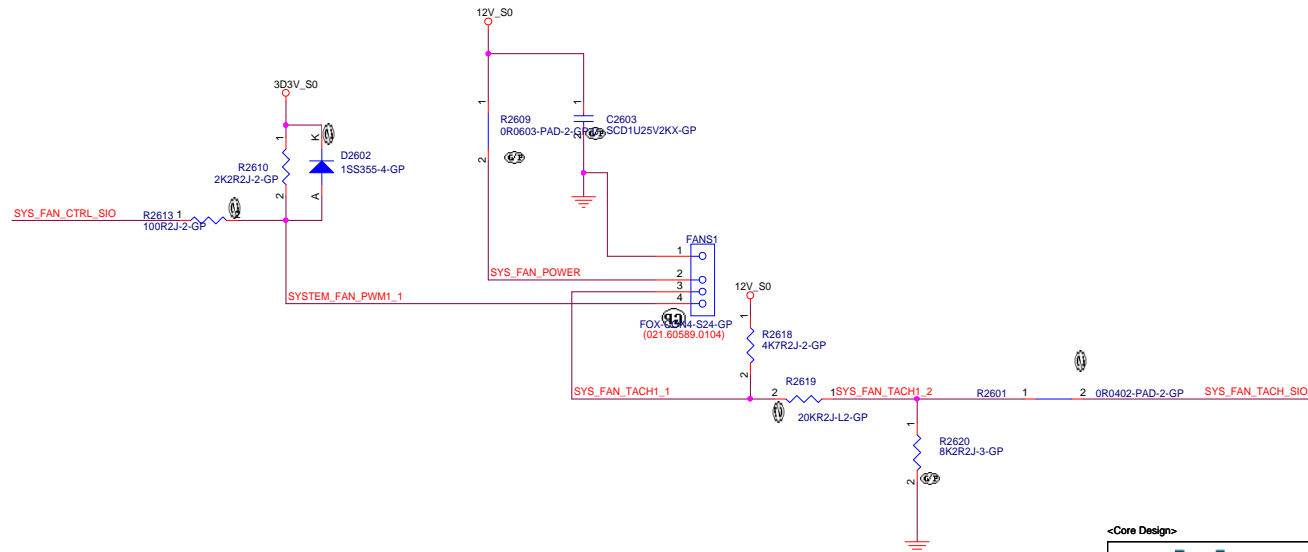
## CPU FAN

24 CPU\_FAN\_CTRL\_SIO >>—  
 24 CPU\_FAN\_TACH\_SIO <<—  
 24 SYS\_FAN\_CTRL\_SIO >>—  
 24 SYS\_FAN\_TACH\_SIO <<—




## SYS FAN

### 4 PINS FAN CONTROL



<Core Design>

		<b>Wistron Incorporated</b> 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>Thermal &amp; FAN</b>			
Size	Document Number		Rev
Customer	<b>vWolverine</b>		-1
Date:	Tuesday, March 21, 2017	Sheet	26 of 107

```

6  HDA_SDINO_CPU
6  HDA_SDOUT_CODEC
6  HDA_RST#_CODEC
6  HDA_SYNC_CODEC
6  HDA_BITCLK_CODEC

```

30 AUD\_IN\_L >>> \_\_\_\_\_

30 AUD\_IN\_R >>> \_\_\_\_\_

30 AUDAMPIN\_L <<< \_\_\_\_\_

30 AUDAMPIN\_R <<< \_\_\_\_\_

30 MIC1\_VREFO\_L <<< \_\_\_\_\_

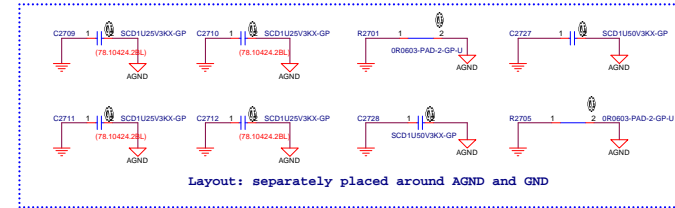
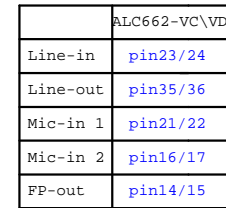
30 AUD\_MIC1\_L >>> \_\_\_\_\_

30 AUD\_MIC1\_R >>> \_\_\_\_\_

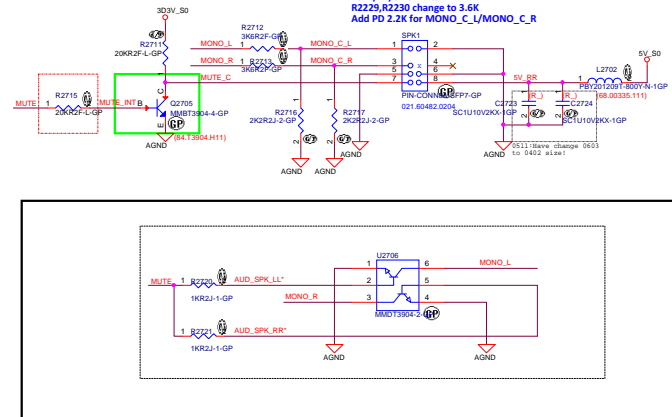
30 MIC1\_VREFO\_R <<< \_\_\_\_\_

30 SENSE\_A >>> \_\_\_\_\_

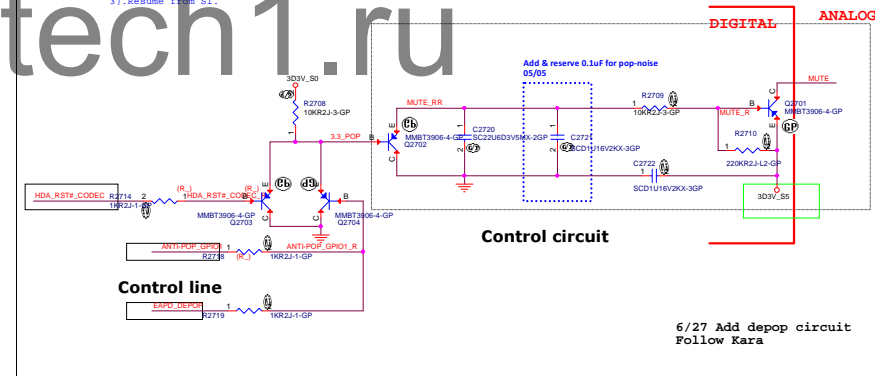
29 SENSE\_B >>—  
29 MIC2\_VREFO >>—  
29 FP\_MIC2\_L >>—  
29 FP\_MIC2\_R >>—  
29 FP\_OUT\_L <<—  
29 FP\_OUT\_R <<—  
29 LINE2\_VREFO >>—  
29,30 MUTE <<—



2014/12/31-SB Vita  
R2229,R2230 change to 3.6K  
Add PD 2.2K for MONO\_C\_L/MONO\_C\_R



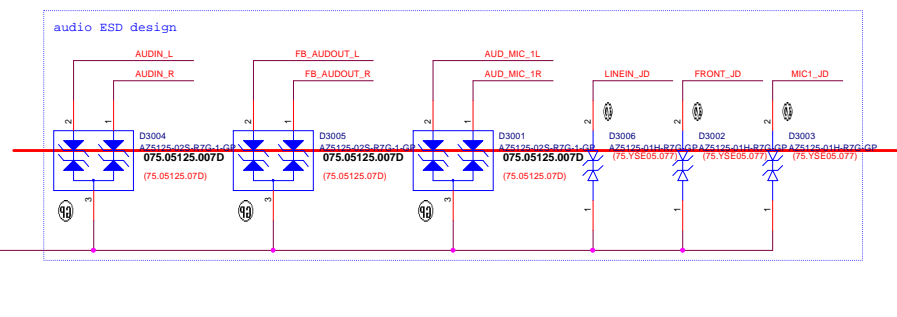
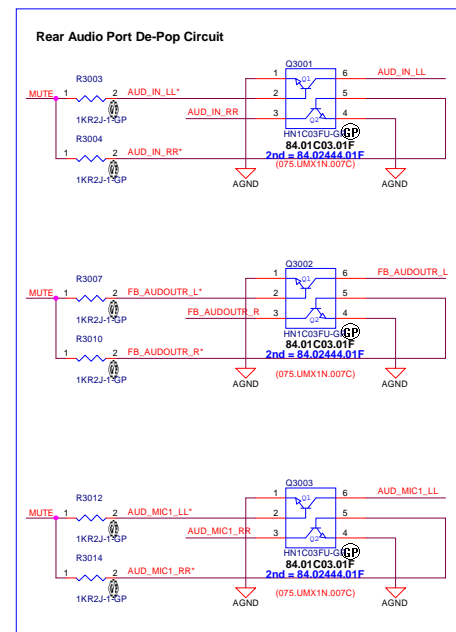
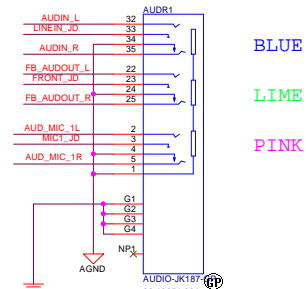
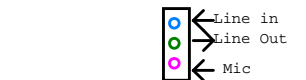
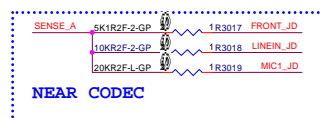
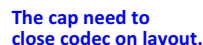
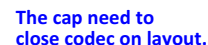
```
Control by software driver and CODEC GPIO.
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.
```

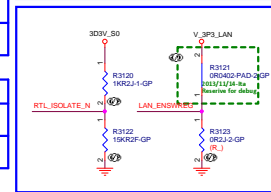
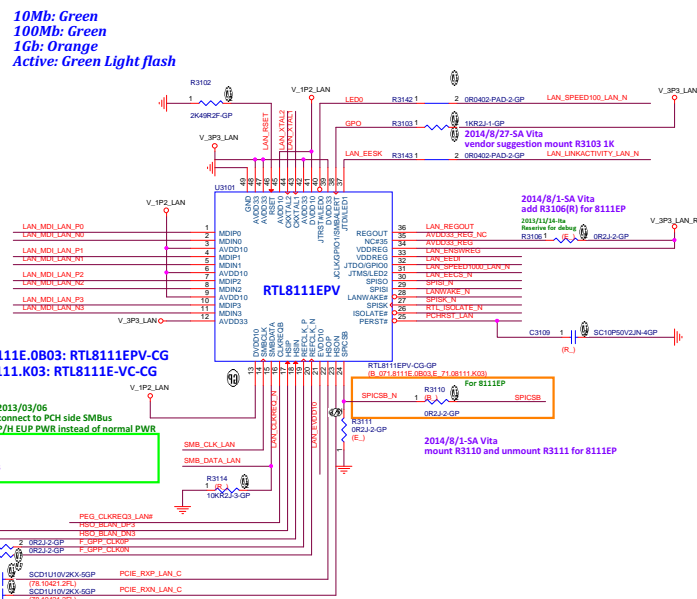
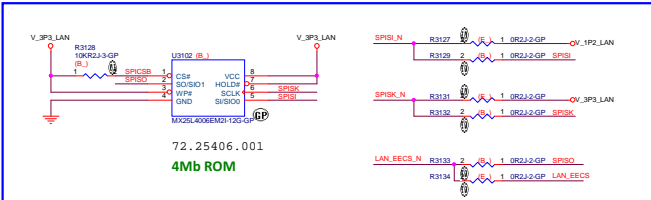
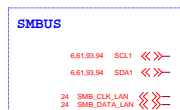


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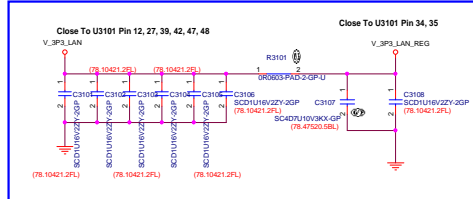
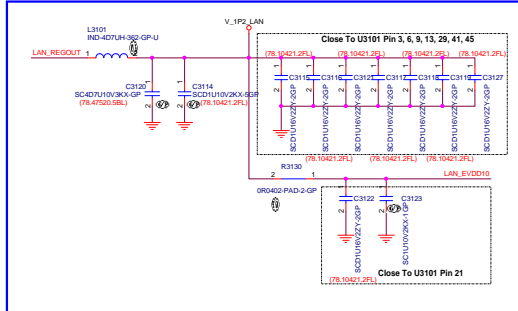


**AUDIO REAR PORT**





Pin35 / VDDREG	Mount	Un-mount
RTL8111EPV		
RTL8111E-VC	R3106	

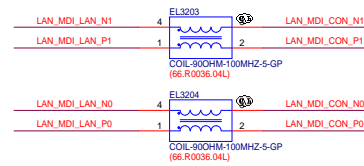
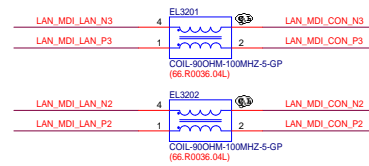


## LAN

31 LAN\_MDI\_LAN\_P0 >>>  
31 LAN\_MDI\_LAN\_N0 >>>  
31 LAN\_MDI\_LAN\_P1 >>>  
31 LAN\_MDI\_LAN\_N1 >>>  
31 LAN\_MDI\_LAN\_P2 >>>  
31 LAN\_MDI\_LAN\_N2 >>>  
31 LAN\_MDI\_LAN\_P3 >>>  
31 LAN\_MDI\_LAN\_N3 >>>  
31 LAN\_SPEED1000\_LAN\_N >>>  
31 LAN\_SPEED100\_LAN\_N >>>  
31.64 LAN\_LINKACTIVITY\_LAN\_N >>>

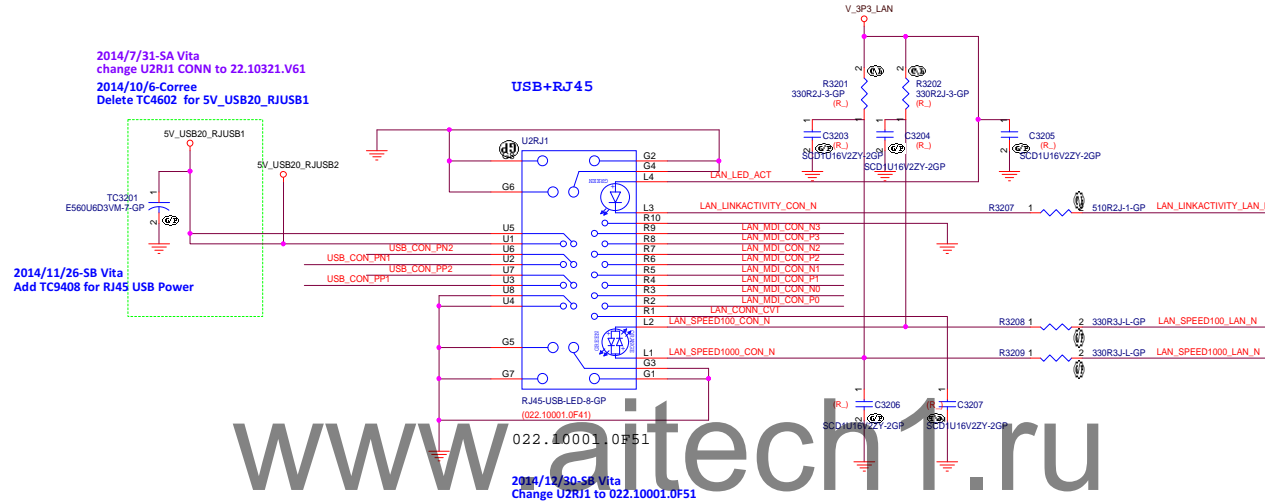
## USB

36 USB\_CON\_PN2 >>>  
36 USB\_CON\_PP2 >>>  
36 USB\_CON\_PN1 >>>  
36 USB\_CON\_PP1 >>>

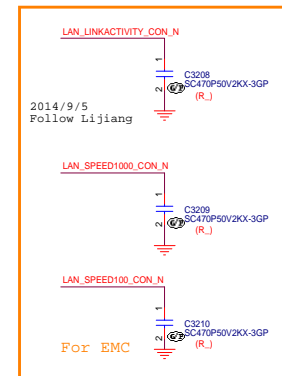
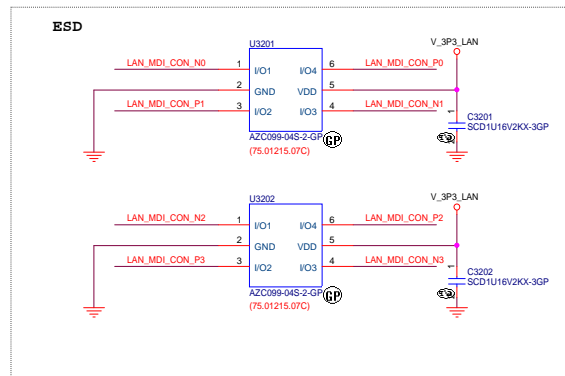


	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

2014/7/31-SA Vita  
change U2RJ1 CONN to 22.10321.V61  
2014/10/6-Corree  
Delete TC4602 for 5V\_USB20\_RJUSB1



## ESD



2014/12/15-SB Vita  
change C3201, C3206, C3208 from 078.47124.02FV to 78.47124.2FL

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<Cell Design>

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Rev (Reserved)		
Doc No	Document Number	Rev
Comp	Wolverine	-1
Date	Wednesday, March 21, 2013	Sheet 35 of 107

## USB 2.0 Rear Signals for RJ45/USB2.0 Stack

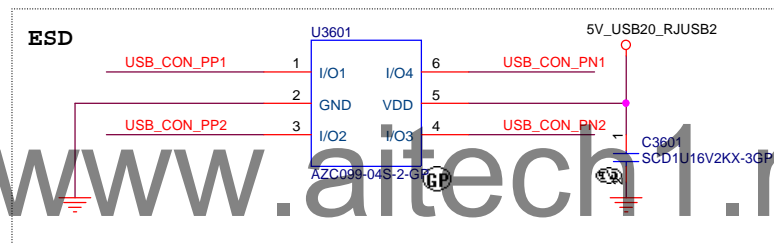
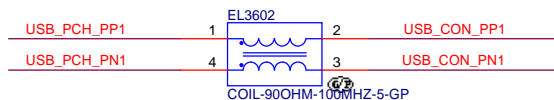
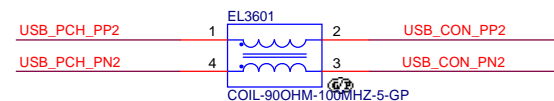
19 USB\_PCH\_PP2  
19 USB\_PCH\_PN2

19 USB\_PCH\_PP1  
19 USB\_PCH\_PN1

32 USB\_CON\_PP2  
32 USB\_CON\_PN2

32 USB\_CON\_PP1  
32 USB\_CON\_PN1

## USB 2.0 Rear Signals for RJ45/USB2.0 Stack



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Title  
**USB 20\_REAR PORT**

Size Document Number  
Custom **vWolverine**

Rev  
-1

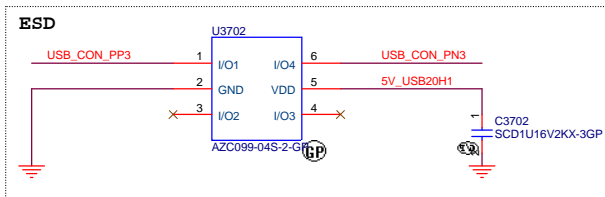
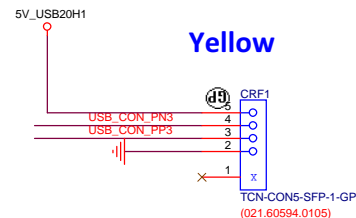
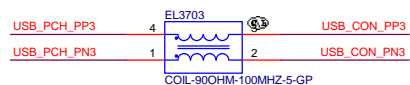
Date: Tuesday, March 21, 2017 Sheet 36 of 107

## CR HEADER

19 USB\_PCH\_PP3  
19 USB\_PCH\_PN3

19 USB\_PCH\_PP12  
19 USB\_PCH\_PN12

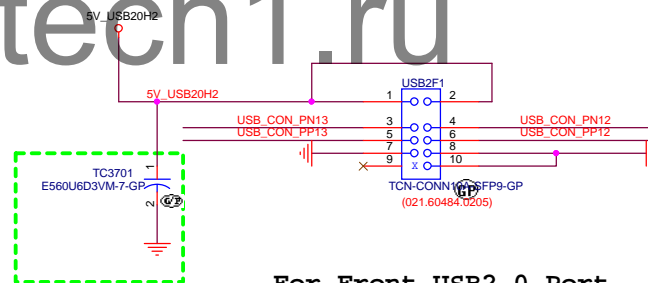
19 USB\_PCH\_PP13  
19 USB\_PCH\_PN13



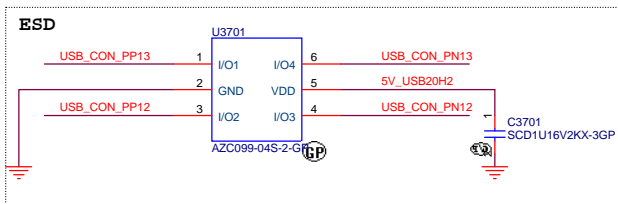
## USB2.0 FRONT HEADER



2014/10/6-Corree  
add TC9407 for 5V\_USB20\_H2 for USB2F1



For Front USB2.0 Port



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Title  
**USB20\_FRONT HEADER**

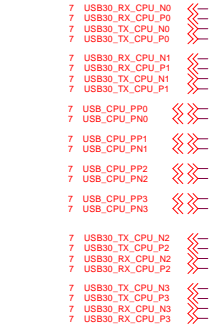
Size  
Custom  
**Wolverine**

Date: Tuesday, March 21, 2017

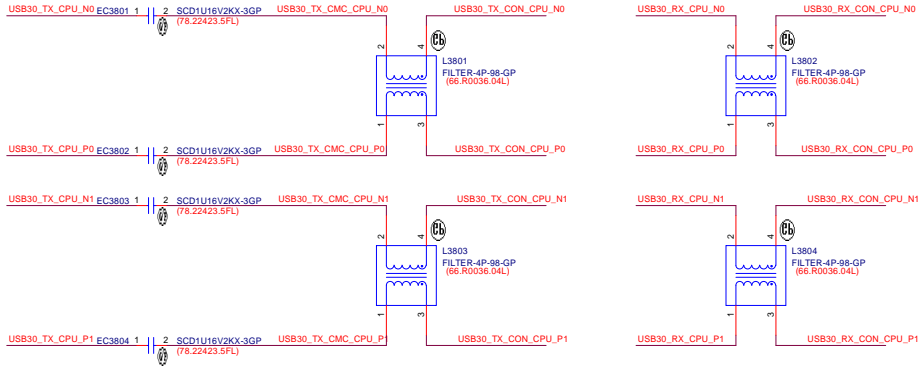
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Rev  
-1

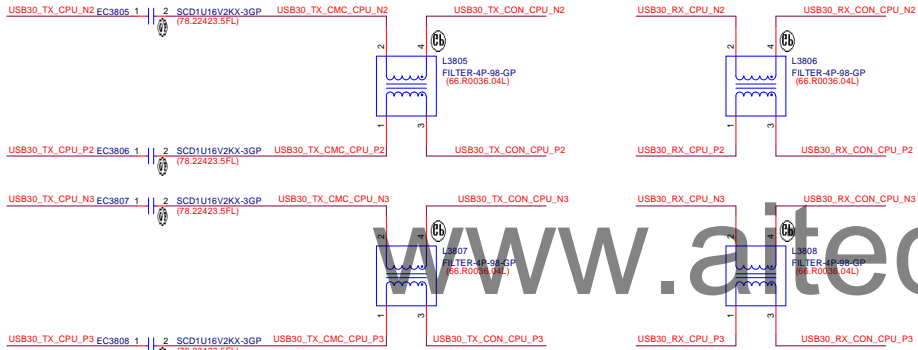
USB3.0 REAR CONNECTOR



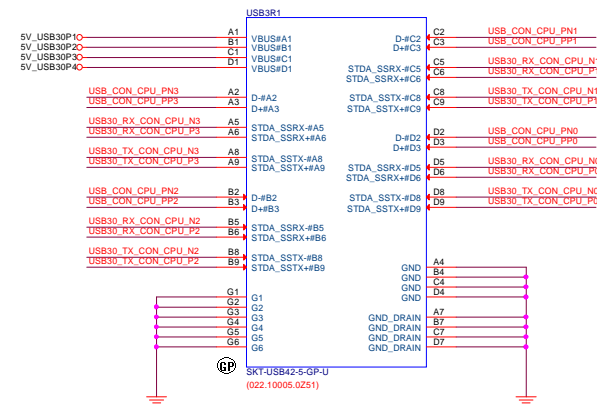
USB3.0 EMI



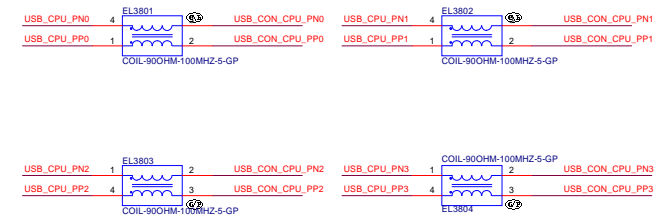
USB3.0 EMI



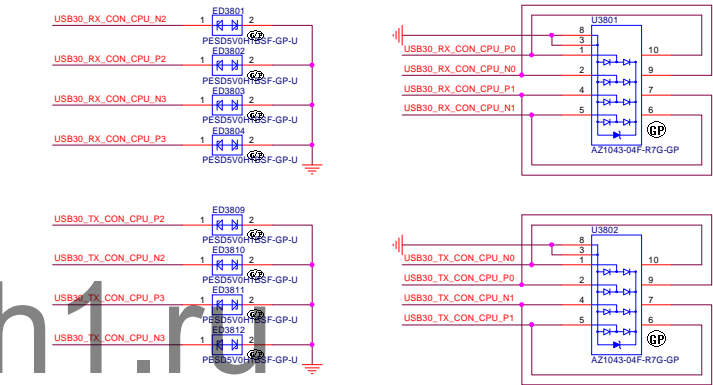
USB3.0 REAR PORT1



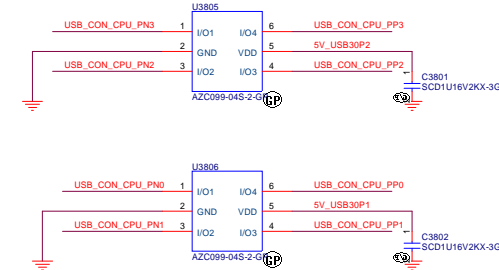
EMI



ESD



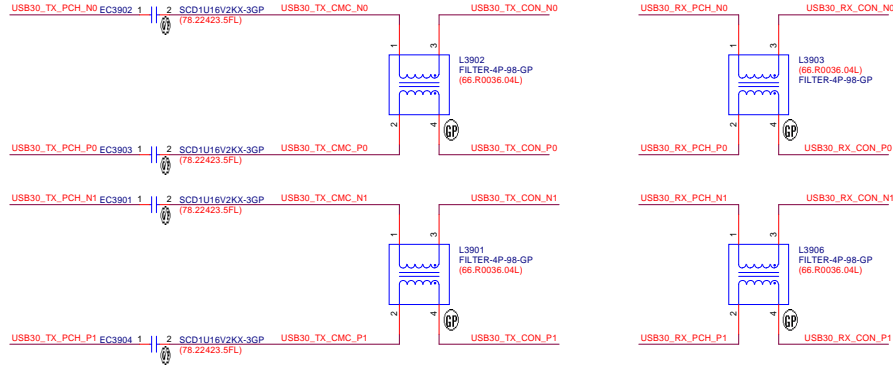
ESD



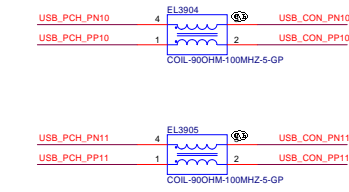
## USB3.0 FRONT HEADER

- 19 USB30\_RX\_PCH\_N0
- 19 USB30\_RX\_PCH\_P0
- 19 USB30\_TX\_PCH\_N0
- 19 USB30\_TX\_PCH\_P0
- 19 USB30\_RX\_PCH\_N1
- 19 USB30\_RX\_PCH\_P1
- 19 USB30\_TX\_PCH\_N1
- 19 USB30\_TX\_PCH\_P1
- 19 USB\_PCH\_PP10
- 19 USB\_PCH\_PP11
- 19 USB\_PCH\_PP11

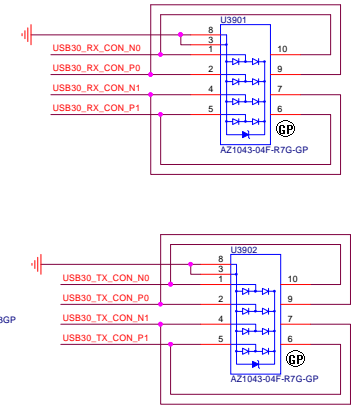
## USB3.0 EMI



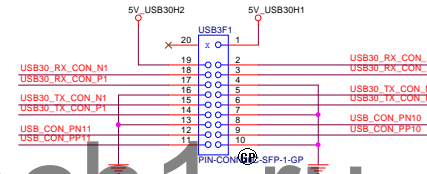
## EMI



## ESD



## USB3.0 FRONT HEADER 1



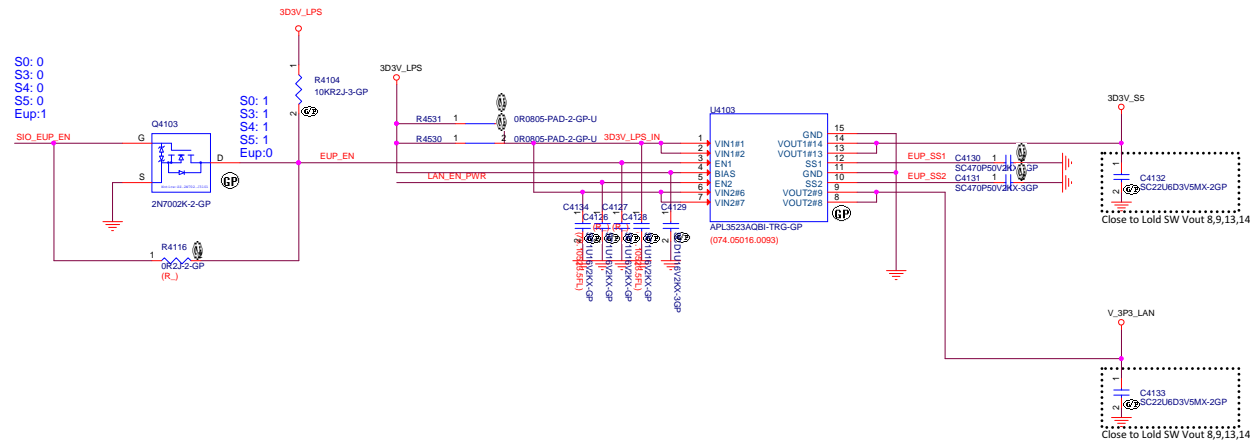
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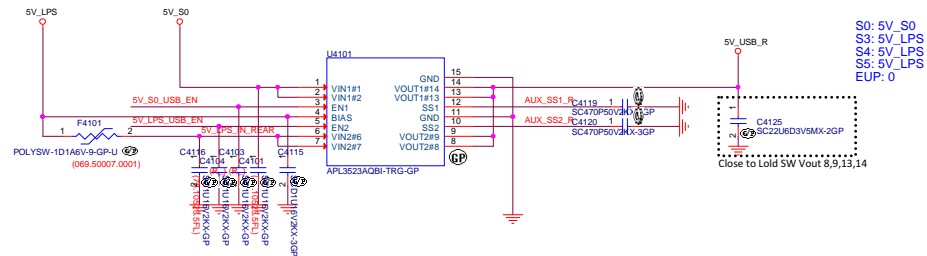
<b>wlstron</b>		<b>Wlstron Incorporated</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsien	
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Size	Document Number		Rev
Customer	<b>Wolverine</b>		-1
Date:	Tuesday, March 21, 2017	Sheet 39 of 107	



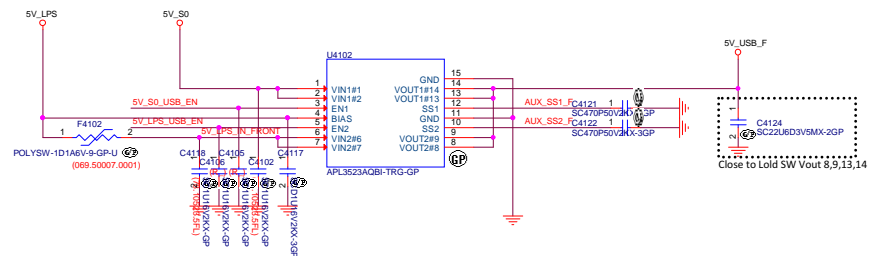
S5\_EuP



## 5V\_USB REAR



## 5V\_USB FRONT

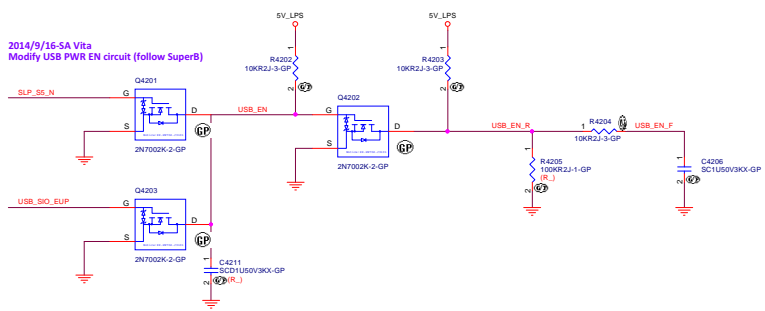




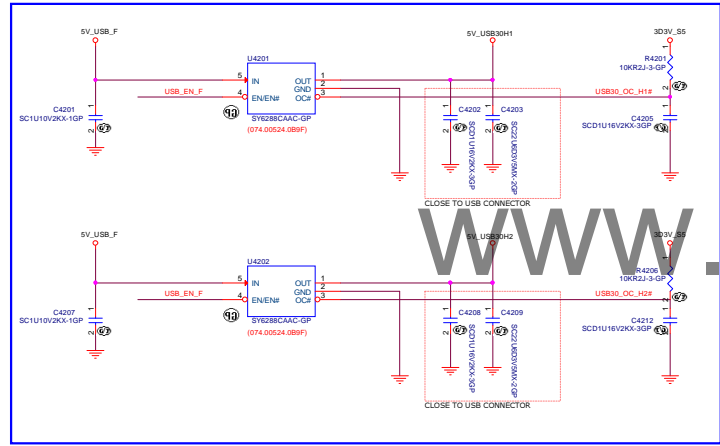
6.24.44.51 SLP\_S5\_N >>  
 24 USB\_SIO\_EUP >>  
 6 USB30\_OC\_R2# <<  
 19 USB30\_OC\_H1# <<  
 19 USB30\_OC\_H2# <<  
 19 USB30\_OC\_H1# <<  
 6.24.43.51.99 SLP\_S3\_N >>

	S5	S4	S3-S0		S5	S4	S3-S0	Status
SLP_S5_N	L	L	H	USB_EN_R	L	L	H	No Support S4/S5 USB wake up
USB_SIO_EUP	L/H	L/H	L	USB_EN_R	L	H	H	Support S4/S5 USB wake up

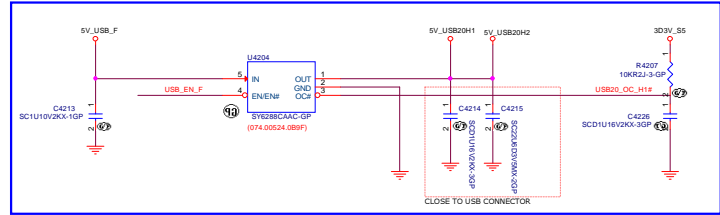
S4, S5 --> choice by USB\_SIO\_EUP  
 S3-S0 --> choice by SLP\_S5\_N



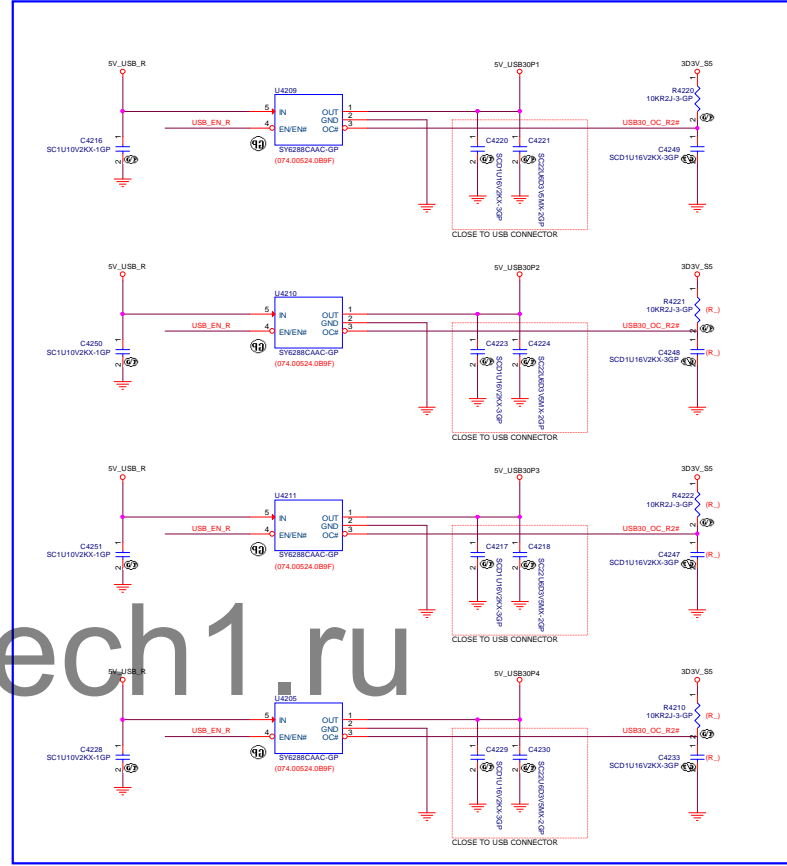
### USB30 HEADER SW (USB3F1)



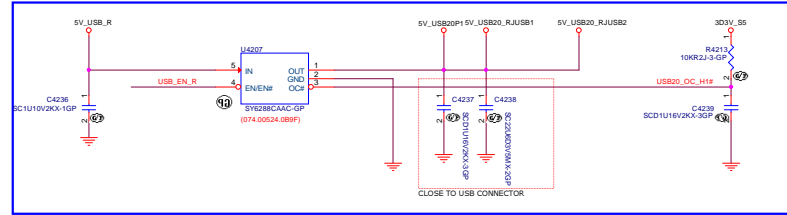
### USB20 PWR FRONT PORT (USB2F1) (CRF1)



### USB30 REAR PORT PWR SW (USB3R1)



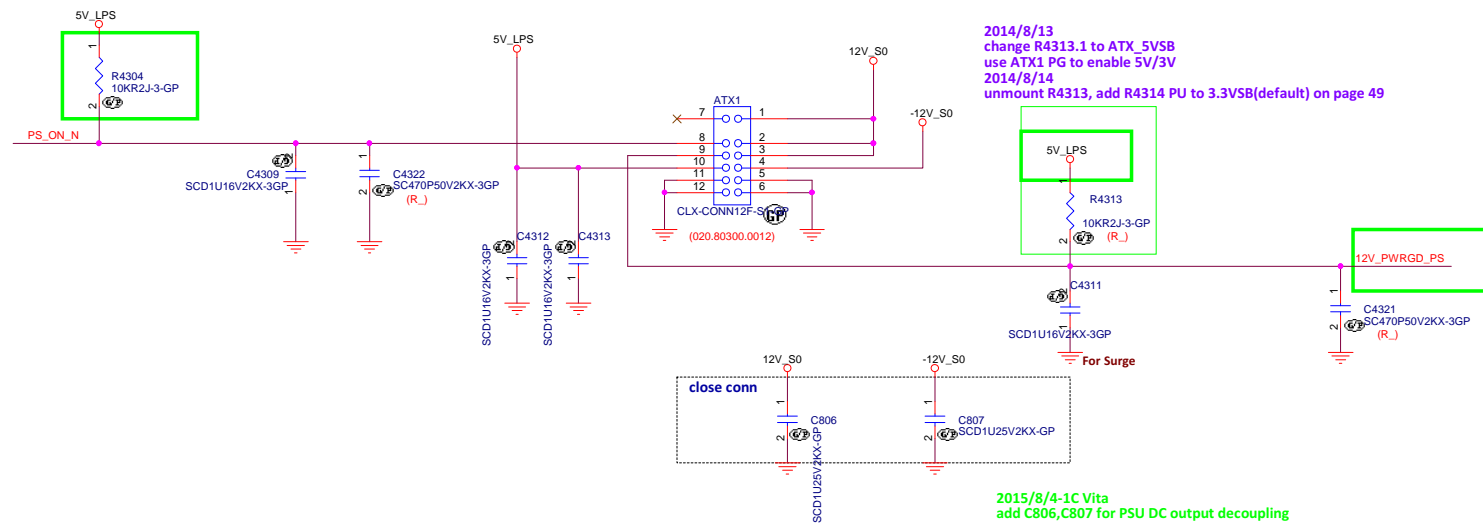
### USB20 PWR REAR PORT (U2RJ1) (PS2)



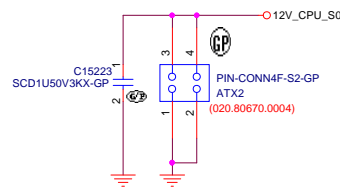
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## ATX CONNECTOR

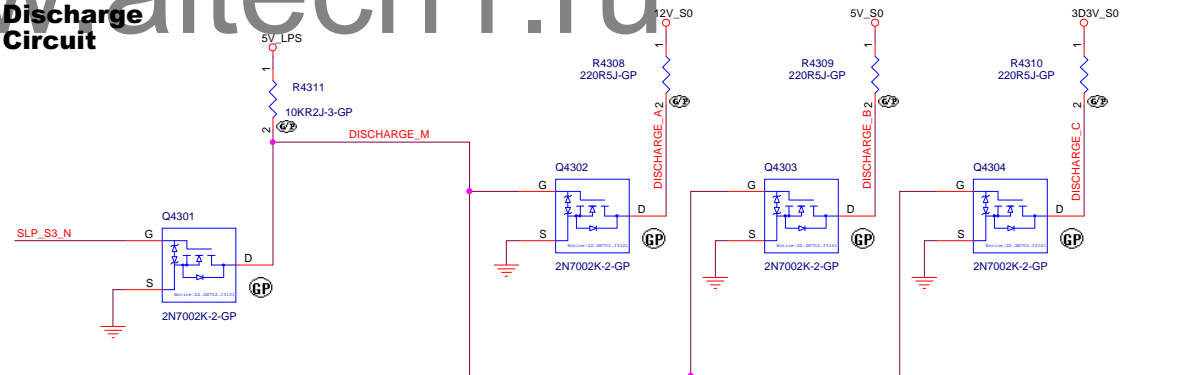
24 PS\_ON\_N >>>  
6,24,51,99 SLP\_S3\_N >>>  
49 12V\_PWRGD\_PS <<<



## CPU PWR CONN



## Discharge Circuit



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Title

ATX

Size

Document Number

Customer

Wolverine

Date

Tuesday, March 21, 2017

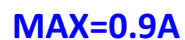
Sheet

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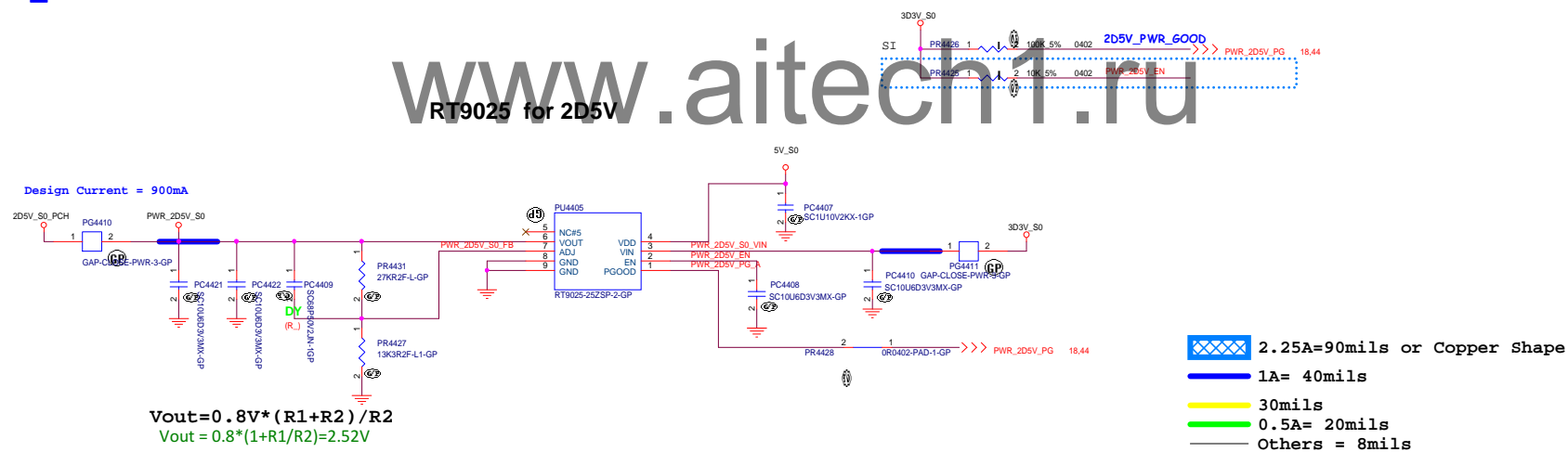
Rev


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**+2D5\_S5**  
**IMax=2.24A**



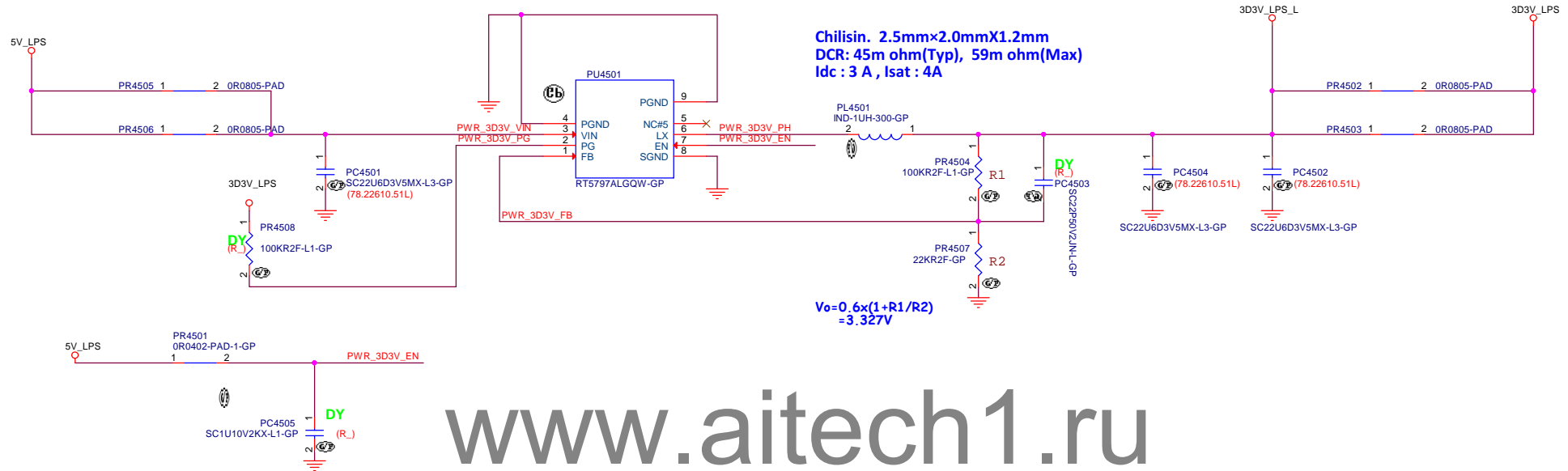
RT9025 for 2D5V



		<b>Wistron Incorporated</b> 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title			
<b>Power Sequence (DDR4)</b>			
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**$V_{in}=5V$**

**Vout=3.3V**  
**I<sub>max</sub>= 2.5A**



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## <Core Design>



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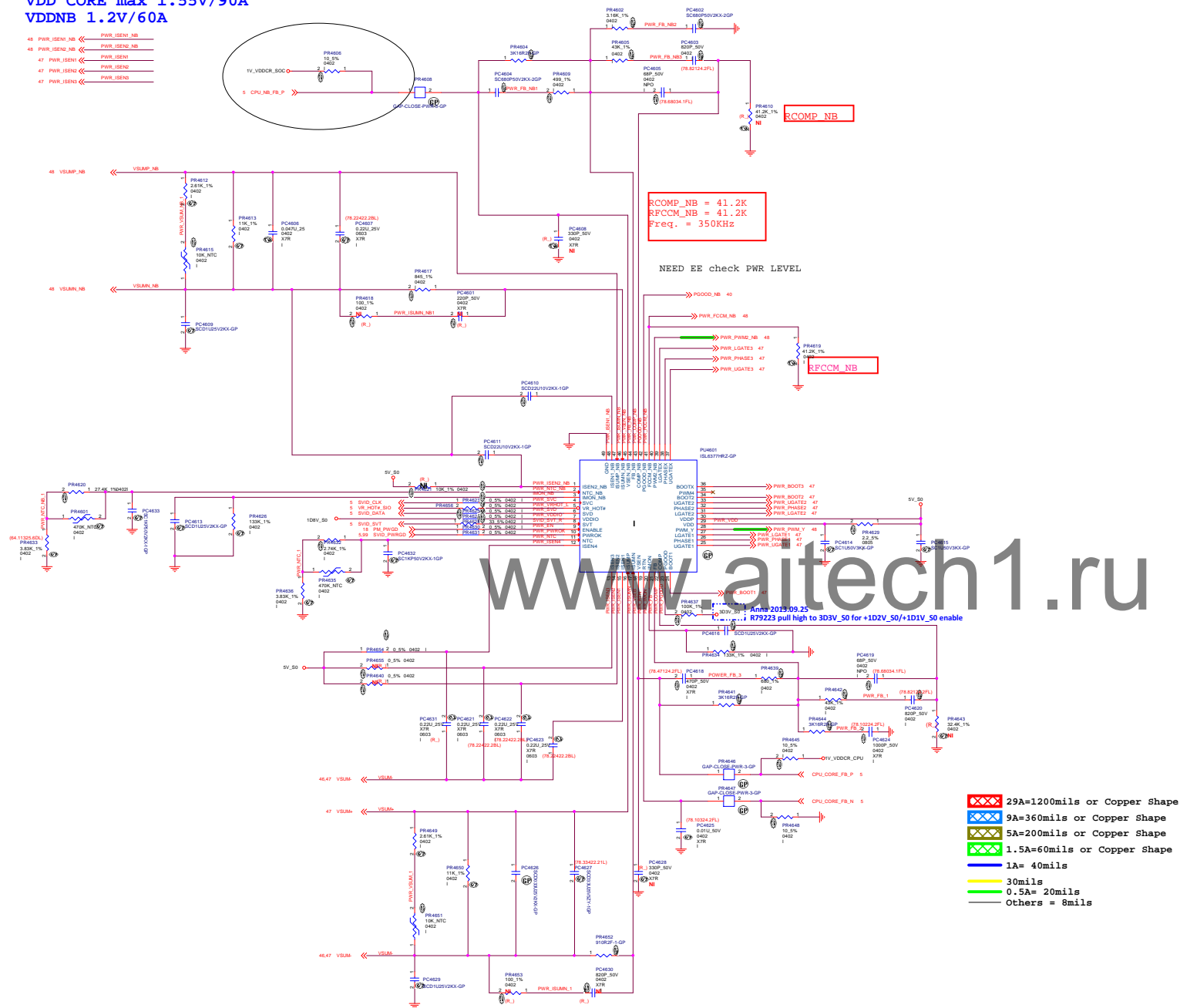
Title **DCDC-3D3V&5V**









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Custom	<b>vWolverine</b>

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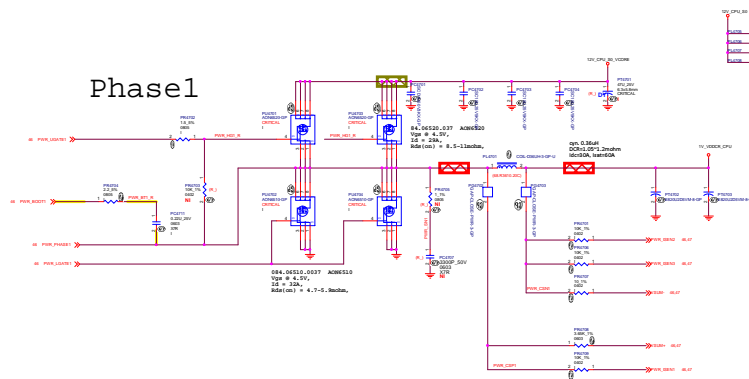
-1

48	PWR_ISEN1_NB	←←	PWR_ISEN1_NB
48	PWR_ISEN2_NB	←←	PWR_ISEN2_NB
47	PWR_ISEN1	←←	PWR_ISEN1
47	PWR_ISEN2	←←	PWR_ISEN2
47	PWR_ISEN3	←←	PWR_ISEN3



	29A=1200mils or Copper Shape
	9A=360mils or Copper Shape
	5A=200mils or Copper Shape
	1.5A=60mils or Copper Shape
	1A= 40mils
	30mils
	0.5A= 20mils
	Others= 8mils

## Phase1

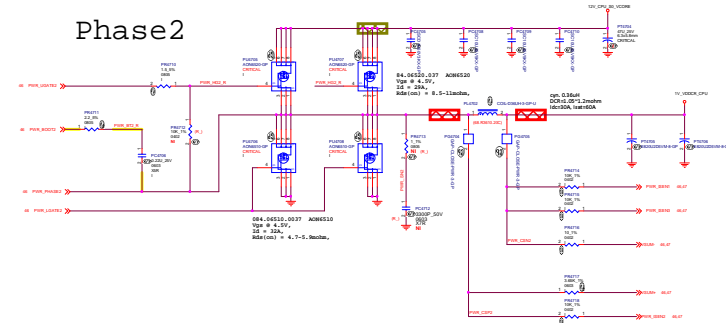


TDC = 65A  
EDC = 95A  
OCP > 110A

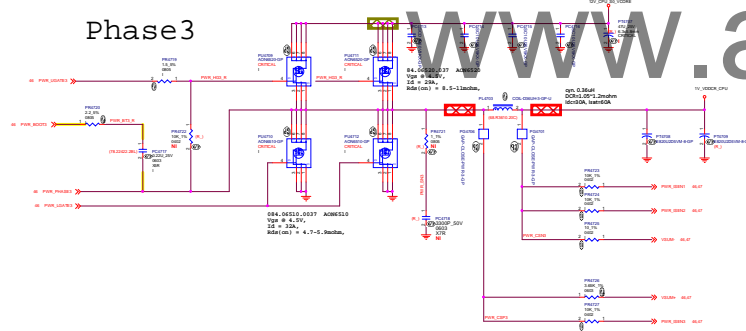
VDD CORE max 1.55V/90A

OVP: If the VSEN voltage exceeds the output voltage VID value plus any programmed offsets by +15mV, the controller declares an overvoltage fault

## Phase2

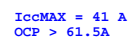


## Phase3

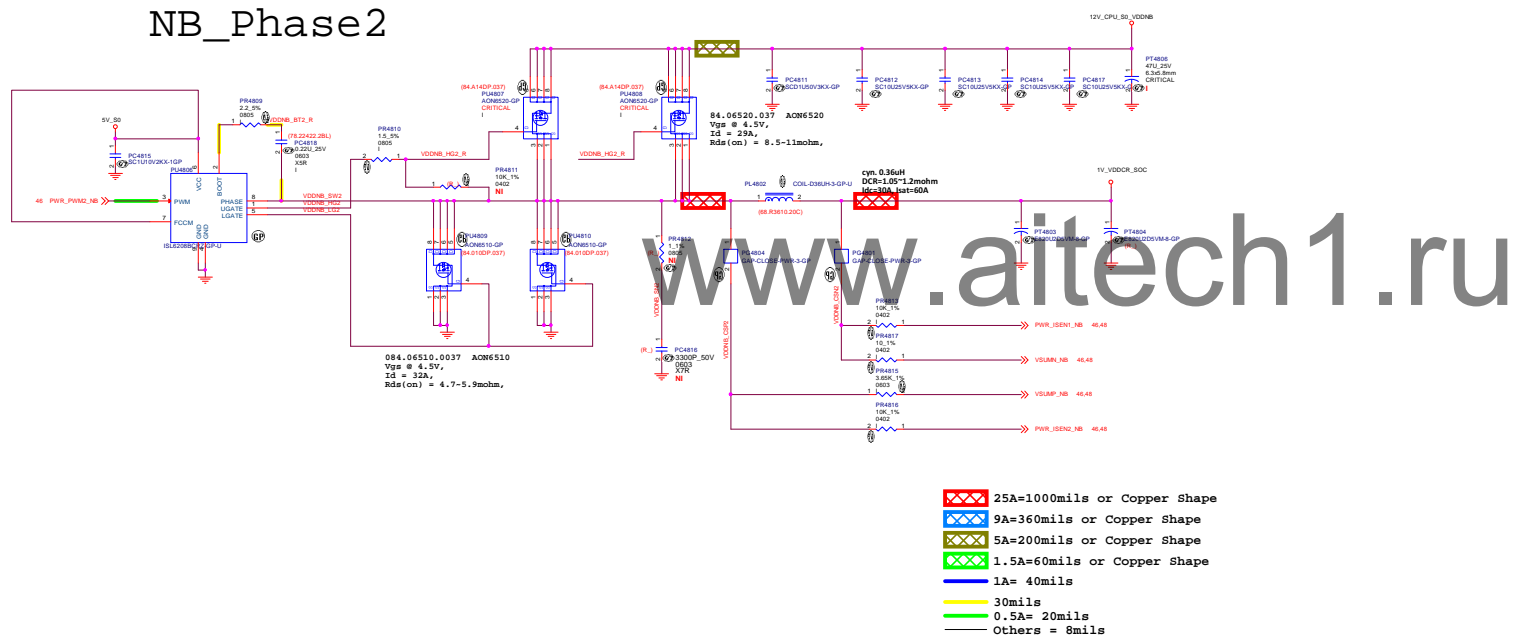



25A=1000mils or Copper Shape  
9A=360mils or Copper Shape  
5A=200mils or Copper Shape  
1.5A=60mils or Copper Shape  
1A= 40mils  
30mils  
0.5A= 20mils  
Others = 8mils

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## NB\_Phase2




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 FAX: +886 (0)2 2658 8889  
 E-MAIL: [service@wistron.com](mailto:service@wistron.com)  
 WWW: [www.wistron.com](http://www.wistron.com)





5



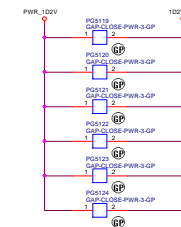
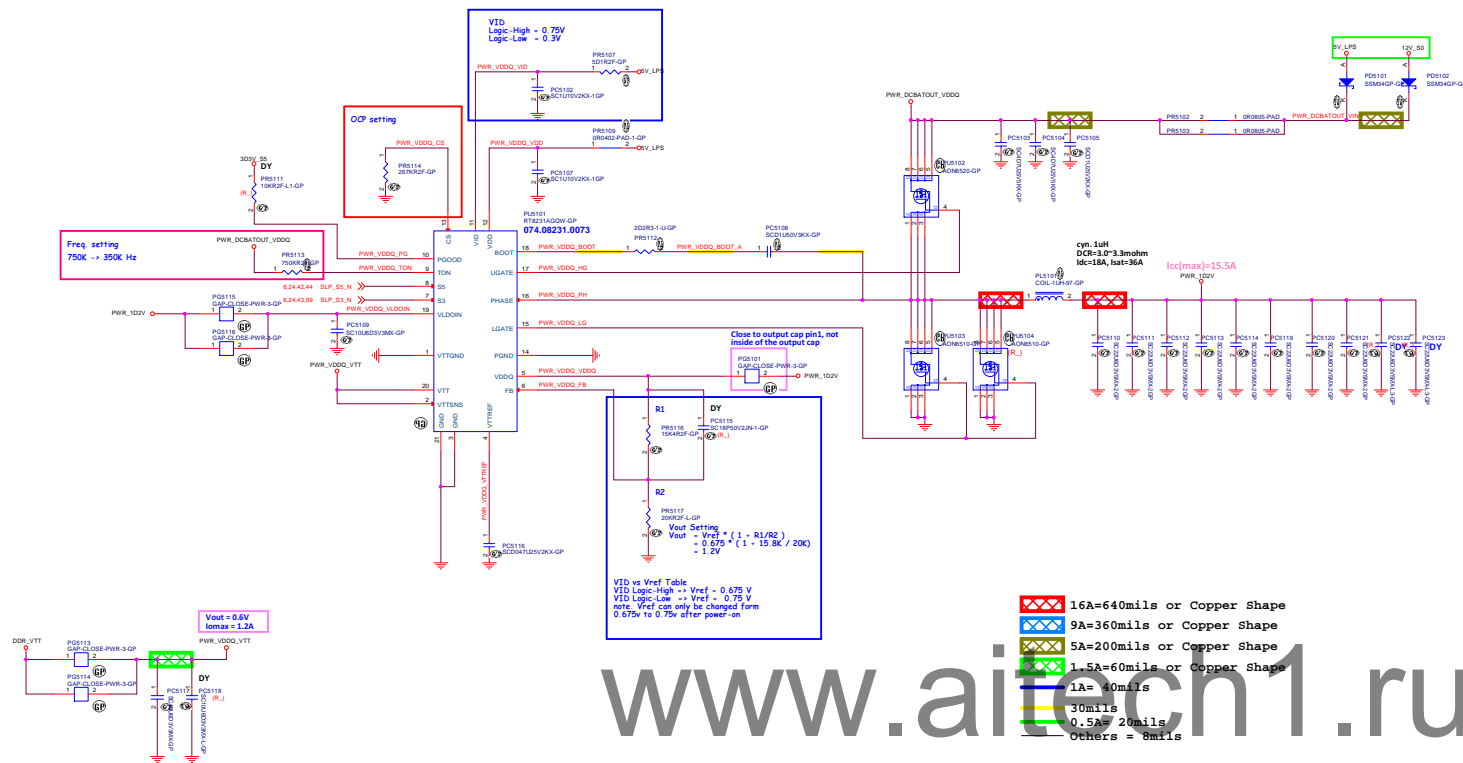
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Date \_\_\_\_\_

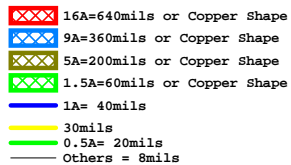
Tuesday, March 21, 2017

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



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## 1D05V & 0D9V CPU



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## 1D05V CHIP SET



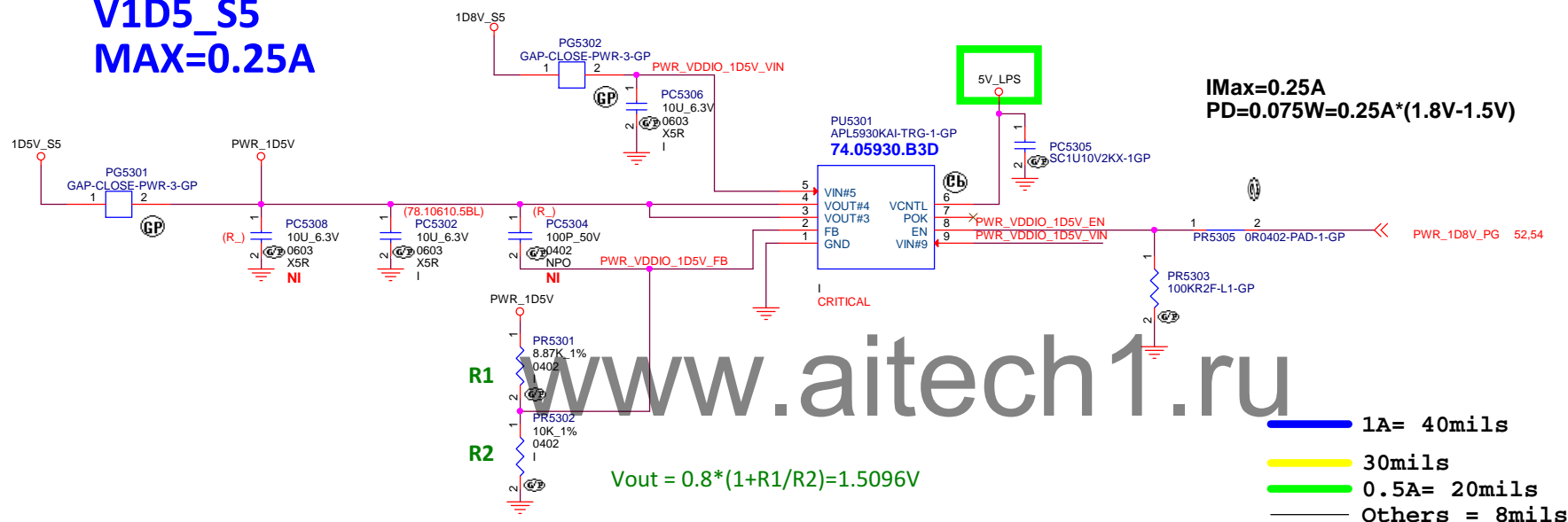
Cyntec: 6.5mm x 6.9mm x 3.0mm  
DCR: 9.0m~10.0mOhm  
Idc : 11 A , Isat : 22 A

**TDC : 8A**

$$\begin{aligned} V_o &= 0.8 \times (1 + R_1/R_2) \\ &= 0.8 \times (1 + 3.16/10) \\ &= 1.05 \end{aligned}$$

**Group A:** 3.3V/5V\_S5-->1.8V\_S5-->0.95V\_S5-->1.5V\_S5

**V1D5\_S5**  
**MAX=0.25A**



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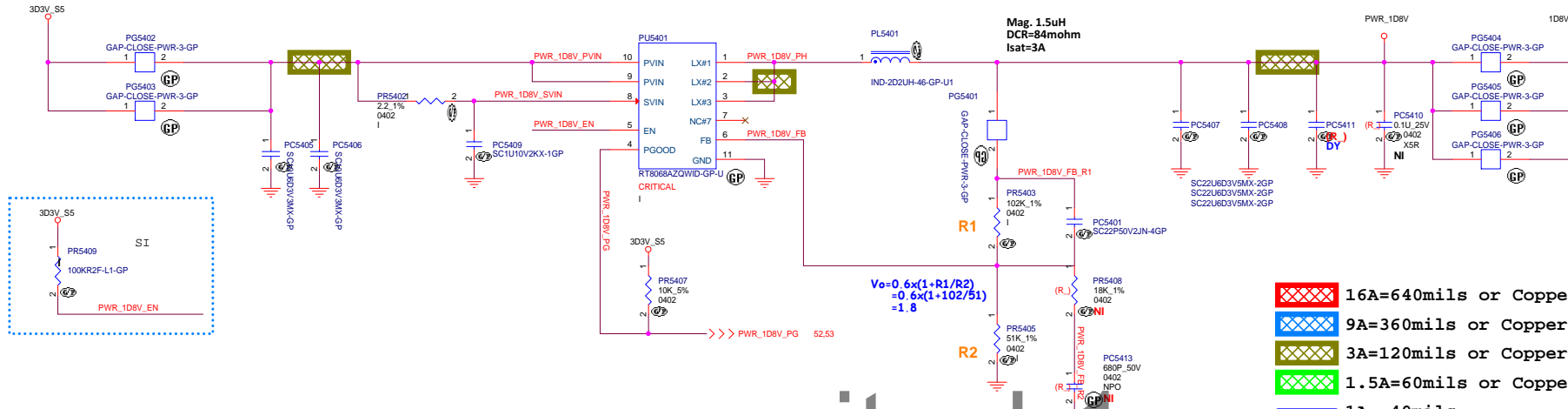
Title	053 DCDC_VDDIO_1D5V_APL5930
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Size B	Document Number <b>vWolverine</b>	Rev -1
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Group A: 5V\_S5/3.3V\_S5 -->1.8V\_S5-->0.95V\_S5-->1.5V\_S5

Imax=2.5A  
OCP>4A  
Frequency=1000KHz



$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 102/51) = 1.8$$

- 16A=640mils or Copper Shape
- 9A=360mils or Copper Shape
- 3A=120mils or Copper Shape
- 1.5A=60mils or Copper Shape
- 1A= 40mils
- 30mils
- 0.5A= 20mils
- Others = 8mils

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Hsinchu, Taipei Hsien

Title: **DCDC\_1D8V\_RT8068**

Size: **Custom** Document Number: **vWolverine** Rev: **-1**

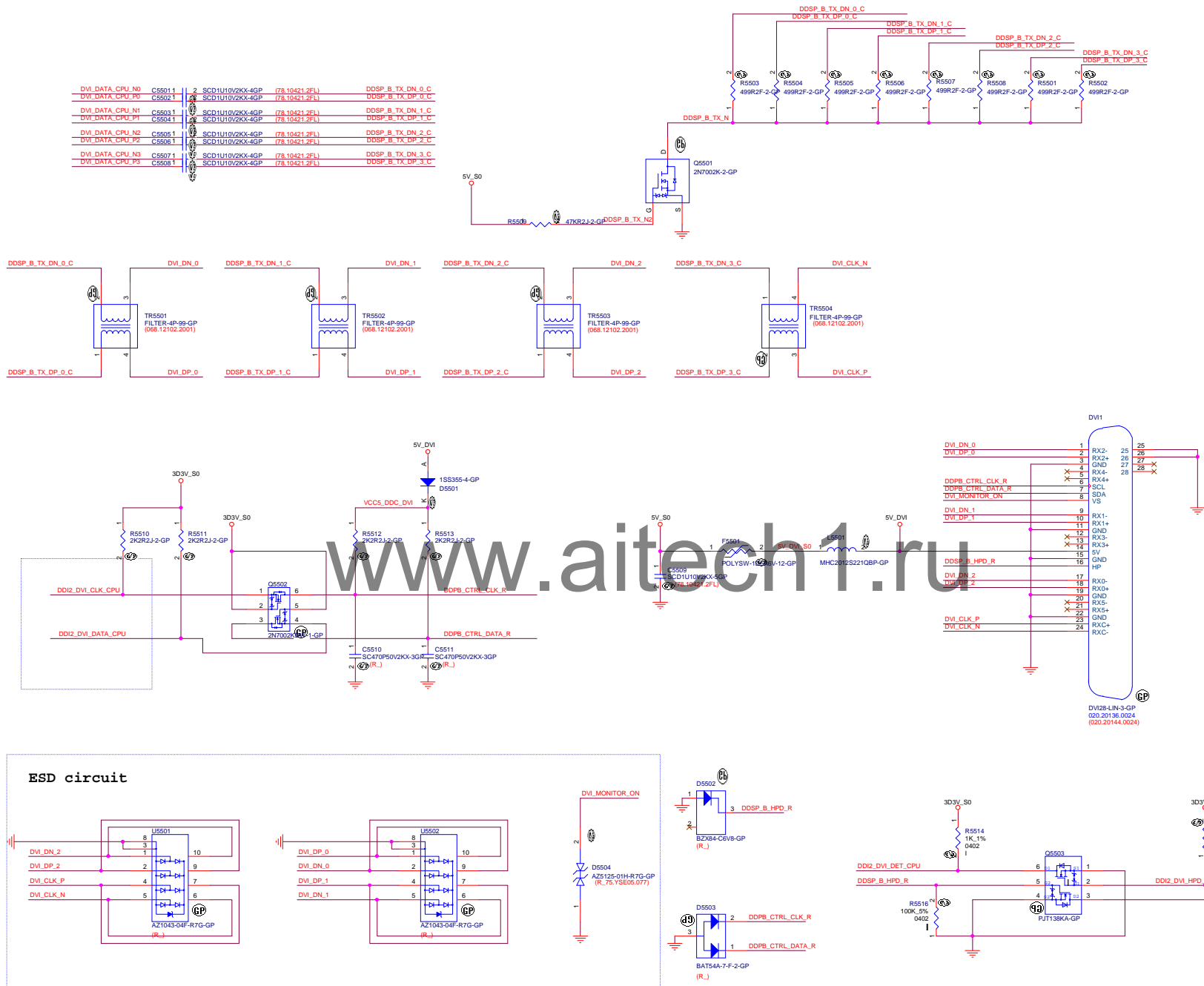
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## DDI2

5 DVI\_DATA\_CPU\_P0  
5 DVI\_DATA\_CPU\_N0  
5 DVI\_DATA\_CPU\_P1  
5 DVI\_DATA\_CPU\_N1  
5 DVI\_DATA\_CPU\_P2  
5 DVI\_DATA\_CPU\_N2  
5 DVI\_DATA\_CPU\_P3  
5 DVI\_DATA\_CPU\_N3  
5 DDI2\_DVI\_CLK\_CPU  
5 DDI2\_DVI\_DATA\_CPU  
5 DDI2\_DVI\_DET\_CPU


## Monitor ON

24 DVI\_MONITOR\_ON



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Title (Reserved)			
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# DP to RTD2166

## For Debug

RTD2166 Slave Address:  
0x64/0x65, 0x68/0x69

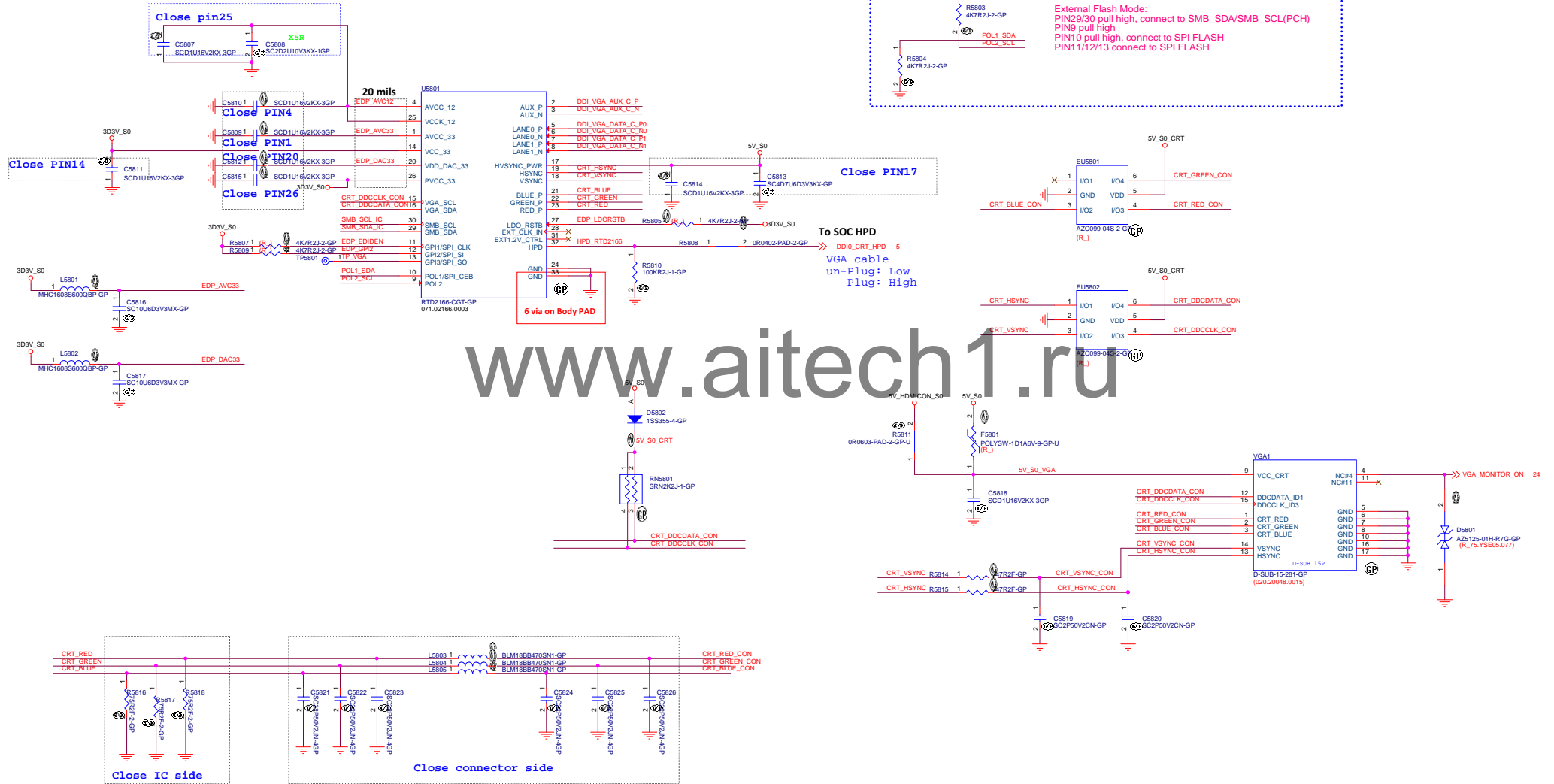
SMB\_SCL\_IC R5801 1 OR0402-PAD-2-GP  
SMB\_SDA\_IC R5802 1 2 OR0402-PAD-2-GP  
SMB\_CLK\_MAIN 6,12,13,14,15  
SMB\_DATA\_MAIN 6,12,13,14,15

## Operation Mode Selection Table(Power on latch)

POL2(PIN9)		POL1_SPIBCE(PIN10)	
		0	1
0	0	Not use, for Internal Test Purpose	Not use, for Internal Test Purpose
	1	ROM MODE	External Flash Mode

ROM Mode:  
PIN29/30 pull high, connect to SMB\_SDA/SMB\_SCL(PCH)  
PIN10 pull down, PIN9 pull high

External Flash Mode:  
PIN29/30 pull high, connect to SMB\_SDA/SMB\_SCL(PCH)  
PIN9 pull high  
PIN10 pull high, connect to SPI FLASH  
PIN11/12/13 connect to SPI FLASH



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Title **CRT**

Size Customer Document Number **Wolverine** Rev 1

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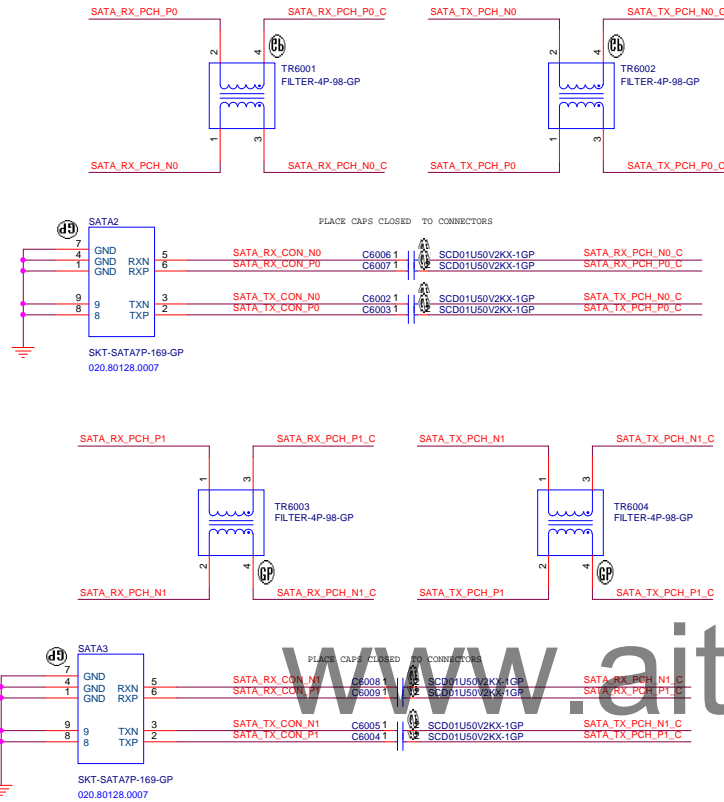
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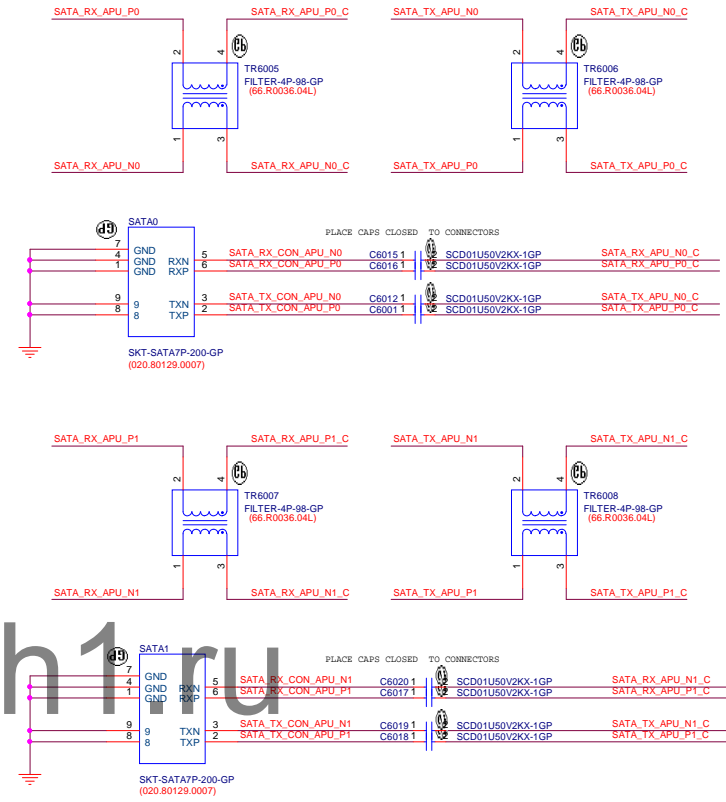
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title (Reserved)			
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- 17 SATA\_TX\_PCH\_N0
- 17 SATA\_TX\_PCH\_P0
- 17 SATA\_RX\_PCH\_N0
- 17 SATA\_RX\_PCH\_P0
- 17 SATA\_TX\_PCH\_N1
- 17 SATA\_TX\_PCH\_P1
- 17 SATA\_RX\_PCH\_N1
- 17 SATA\_RX\_PCH\_P1
- 3 SATA\_TX\_APU\_N0
- 3 SATA\_TX\_APU\_P0
- 3 SATA\_RX\_APU\_N0
- 3 SATA\_RX\_APU\_P0
- 3 SATA\_TX\_APU\_N1
- 3 SATA\_TX\_APU\_P1
- 3 SATA\_RX\_APU\_N1
- 3 SATA\_RX\_APU\_P1

## PCH SATA Port



## APU SATA Port



## SATA Power Conn

2014/11/18-5B Vita  
modify PWR CONN pin define follow Brian



<Core Design>

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File			
HDD/ODD			
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## USB

19 USB\_PCH\_PP4 <<>>  
19 USB\_PCH\_PN4 <<>>

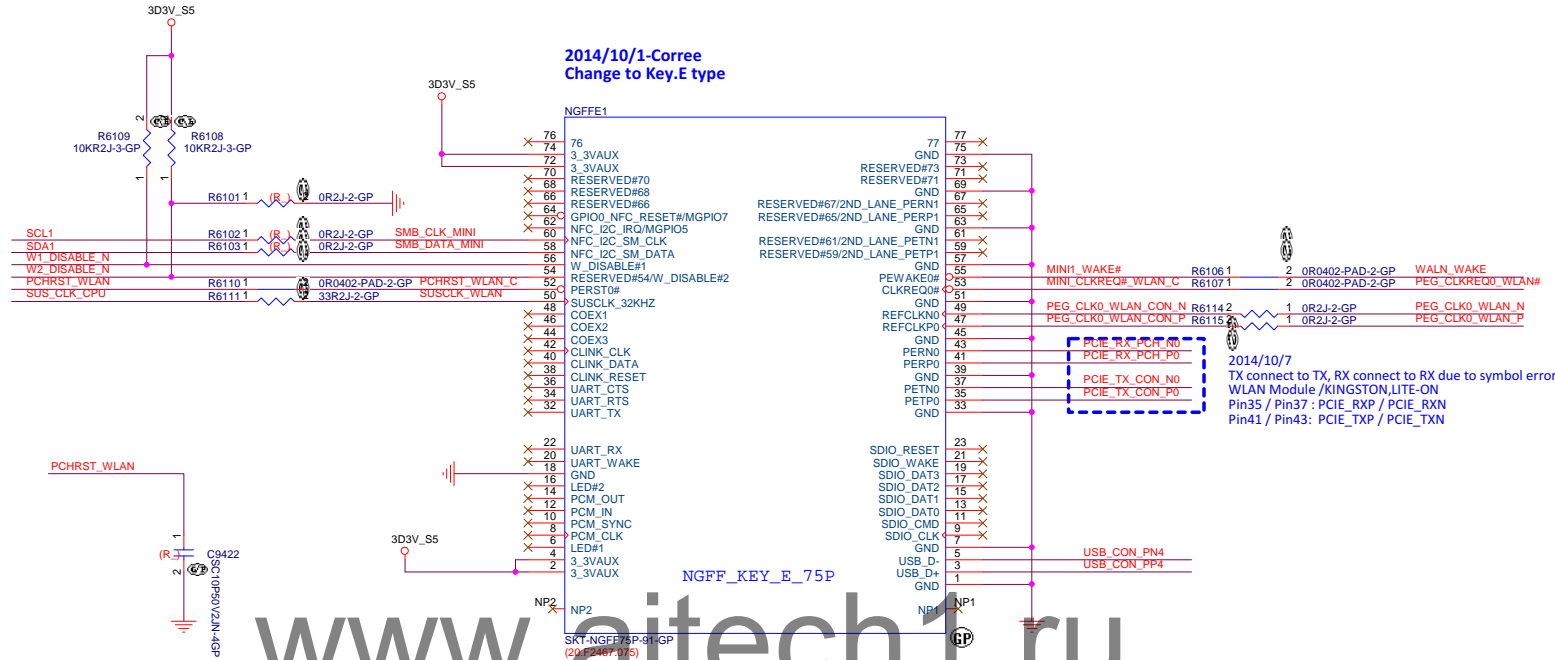
## PCIEX1

17 PCIE\_RX\_PCH\_N0 <<>>  
17 PCIE\_RX\_PCH\_P0 <<>>  
17 PCIE\_TX\_CON\_N0 <<>>  
17 PCIE\_TX\_CON\_P0 <<>>  
19 PEG\_CLK0\_WLAN\_P <<>>  
19 PEG\_CLK0\_WLAN\_N <<>>

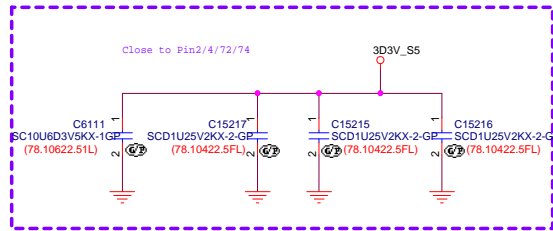
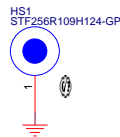
## OTHERS

6 WALN\_WAKE <<>>  
18,61 PCHRST\_WLAN <<>>  
19 PEG\_CLKREQ0\_WLAN# <<>>  
6,31,93,94 SCL1 <<>>  
6,31,93,94 SDA1 <<>>  
6 W1\_DISABLE\_N <<>>  
6 W2\_DISABLE\_N <<>>  
18,61 PCHRST\_WLAN <<>>  
6,16 SUS\_CLK\_CPU <<>>

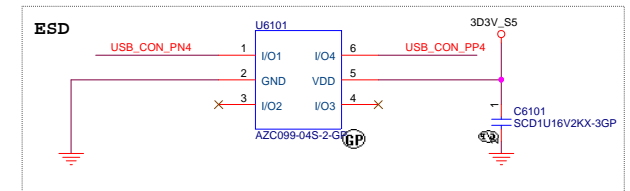
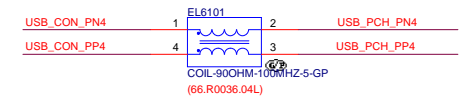
# M.2 2230 / 1630 Key E Type



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2014/12/25-SB Vita  
add F7 (78.10422.5FL) for C6110,C6112,C6113 -- MLCC unify



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Hsichih, Taipei Hsien

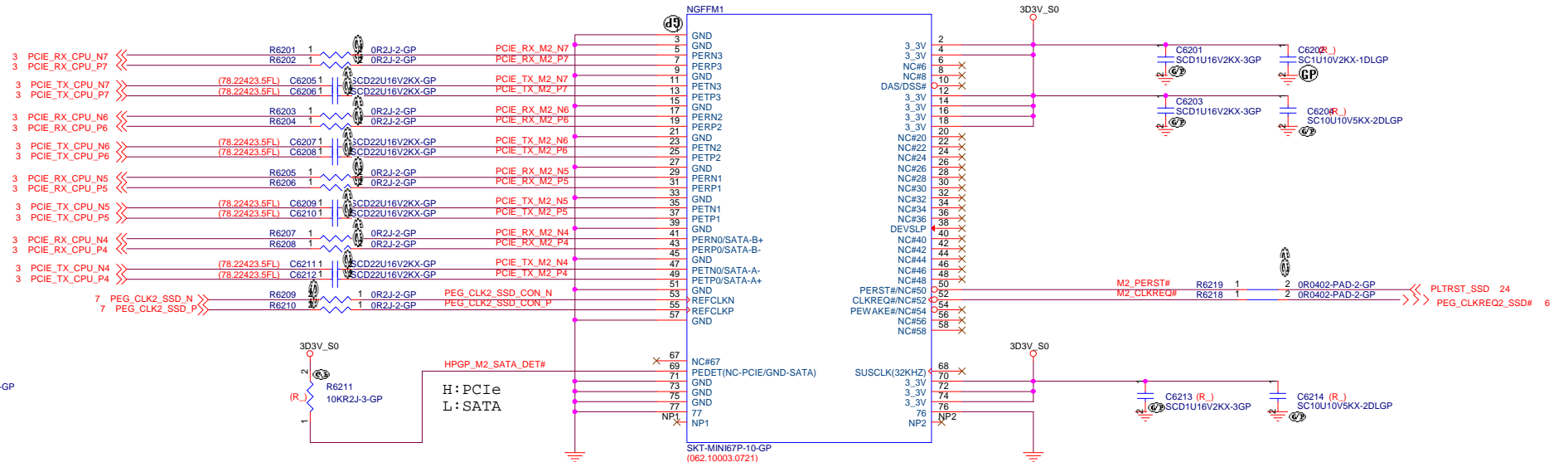
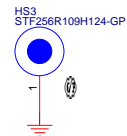
Title **M.2 \_(WLAN)\_Key A**

Size Customer Document Number  
**vWolverine**

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# NGFF(M Key)



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Title  
**M.2 SSD Key M**

Size  
Customer **Wolverine**

Rev  
**-1**

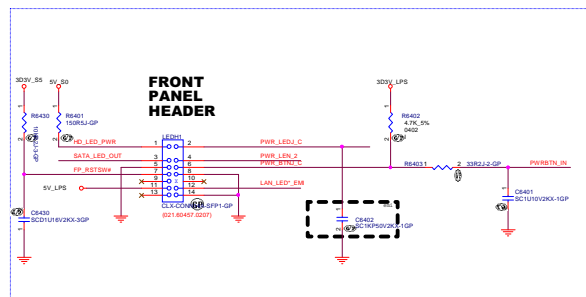
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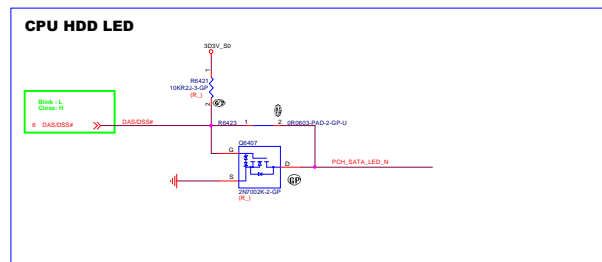
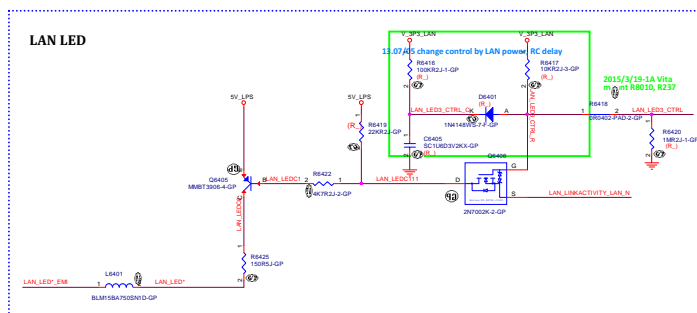
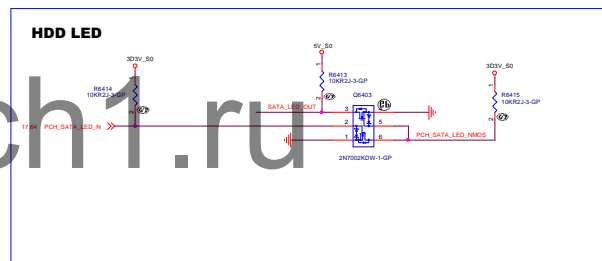
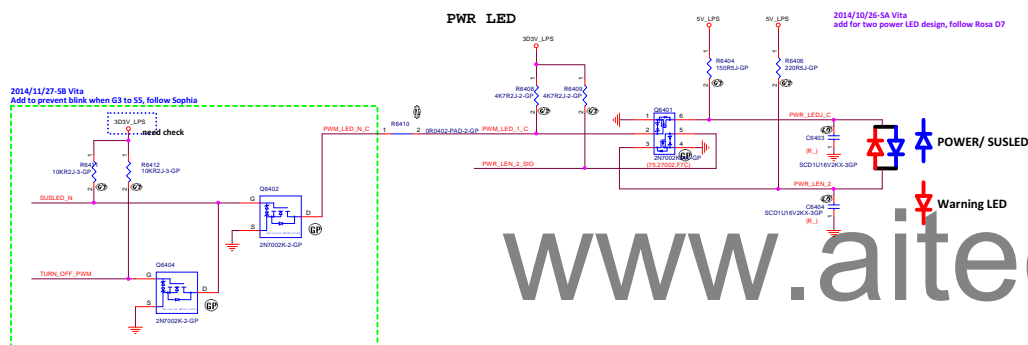
		<b>Wistron Incorporated</b> 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title <b>(Reserved)</b>			
Size A	Document Number <b>vWolverine</b>		Rev -1
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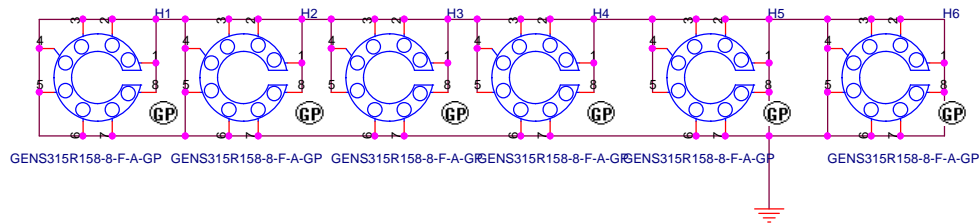
- 4 PP\_RSTSW >>
- 24 SUSLED\_N >>
- 24 PWR\_LEN\_2\_SIO >>
- 17.64 PCH\_SATA\_LED\_N >>
- 24 PWRBTN\_IN <<
- 24 LAN\_LED\_CTRL >>
- 31.32 LAN\_LINKACTIVITY\_LAN\_N >>
- 24 TURN\_OFF\_PWM >>



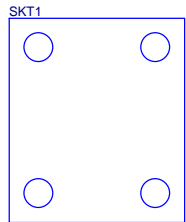
	S0	S0 / Warning	S3	S3 / Warning	S4	S5
SUSLED_N	HIGH	LOW	H & L Circling (Blink)	LOW	HIGH	LOW
PWR_LEN_2_SIO	HIGH	H & L Circling (Blink)	HIGH	H & L Circling (Blink)	LOW	HIGH

System State/Health	Indicator Behavior
S0/ Good	Blue
S0/ Warning or	Blink Red
S3/ Good	Blink Blue
S3/ Warning or	Blink Red
S4	No light
S5	No light





CPU Back Plate



Back Plate (60.3BV09.001)  
CRITICAL

LABEL



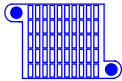
LBL1 LABEL W30\*H10  
(40.3BZ23.011)

Battery Symbol



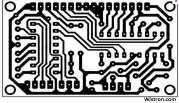
BATT BATTERY CR2032 23.20068.001 KTS 88BCR2032BX  
(23.20068.001) 23.20023.311 MITSUBISHI CR2032 MITSUBISHI  
23.22063.001 JHT CR2032 JHT

HeatSink Symbol



PCHHS1 HEATSINK Vendor  
(334.08901.0001) P/N:  
60.3ET05.001  
60.3ET05.021

PCB Symbol




PCB PCB  
(R\_348.02802.0011)

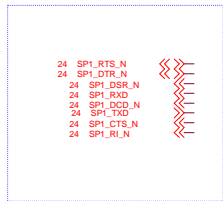
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Title Others		
Size B	Document Number vWolverine	Rev -1
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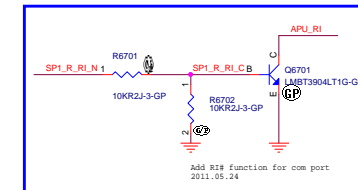
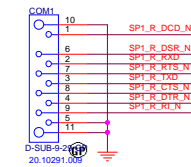
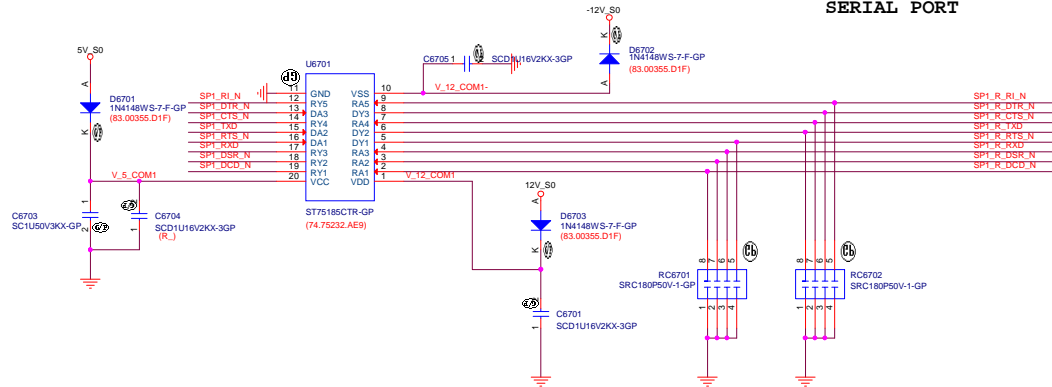
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Title (Reserved)	
Size C	Document Number vWolverine
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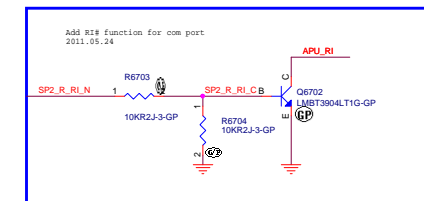
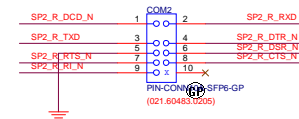
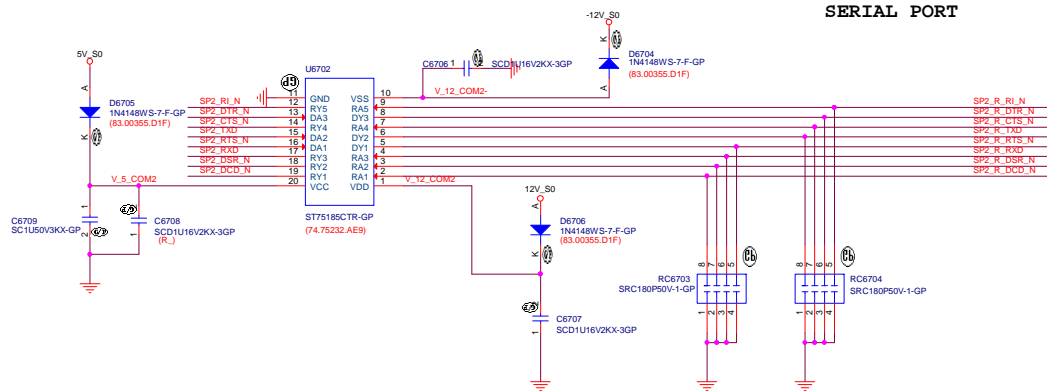
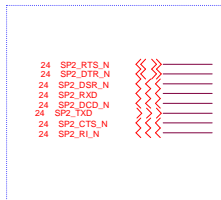
# COM1



6 APU\_RI <<<



# COM2



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Hsinchu, Taipei, Taiwan

Title  
**COM PORT**

Size Document Number

Created by **Wolverine**

Date: Tuesday, March 21, 2017

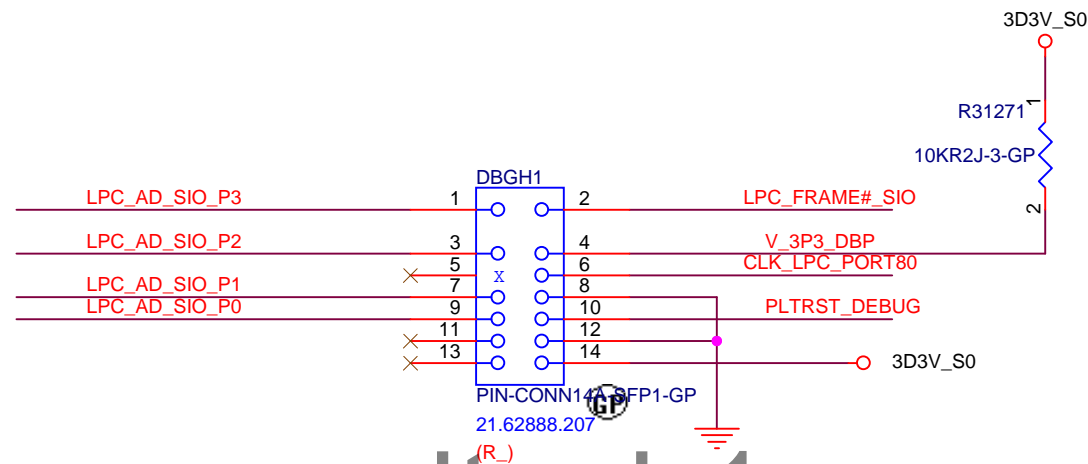
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Rev

1

80 port

Layout close to SIO



www.aitech1.ru Annie pin define

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Hsichih, Taipei Hsien

Title

**Debug port**

Size

A

Document Number

**vWolverine**

Rev

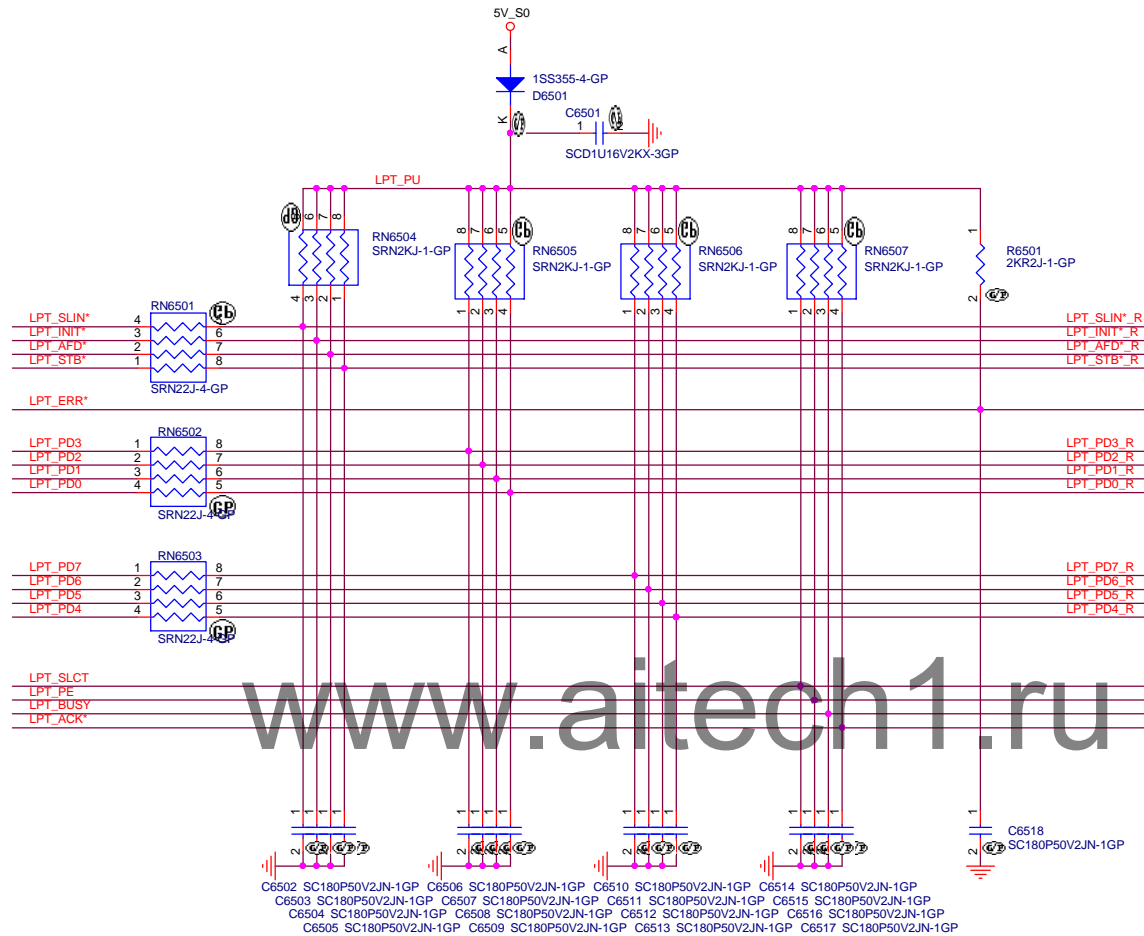
-1

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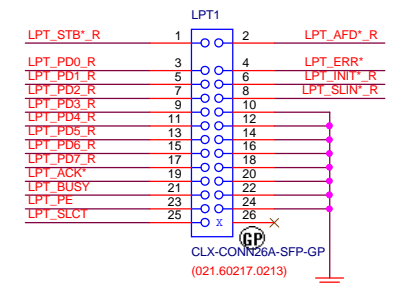
## PARALLEL PORT

24 LPT\_SLCT  
 24 LPT\_PE  
 24 LPT\_BUSY  
 24 LPT\_ACK\*  
 24 LPT\_SLIN\*  
 24 LPT\_ERR\*  
 24 LPT\_AFD\*  
 24 LPT\_STB\*  
 24 LPT\_INIT\*  
 24 LPT\_PD[7:0]



2014/9/11  
 change LPT1 to 021.60217.0213

## LPT




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 Hsichih, Taipei Hsien

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Title (Reserved)	
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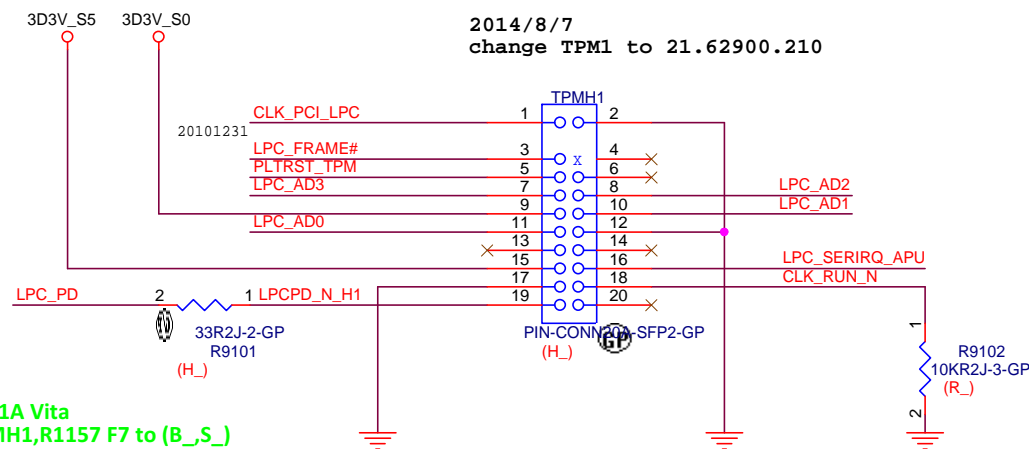
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7,16,24,68 LPC\_FRAME#\_SIO <<>> LPC\_FRAME#  
 7,68 CLK\_LPC\_PORT80 <<>> CLK\_PCI\_LPC  
 24 PLTRST\_TPM <<>> PLTRST\_TPM  
 7,24,68 LPC\_AD\_SIO\_P3 <<>> LPC\_AD3  
 7,24,68 LPC\_AD\_SIO\_P2 <<>> LPC\_AD2  
 7,24,68 LPC\_AD\_SIO\_P1 <<>> LPC\_AD1  
 7,24,68 LPC\_AD\_SIO\_P0 <<>> LPC\_AD0  
 7 LPC\_PD <<>>  
 7,24 LPC\_SERIRQ\_APU <<<

## TPM 2.54 pitch Header



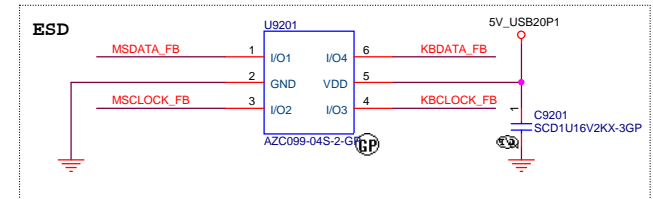
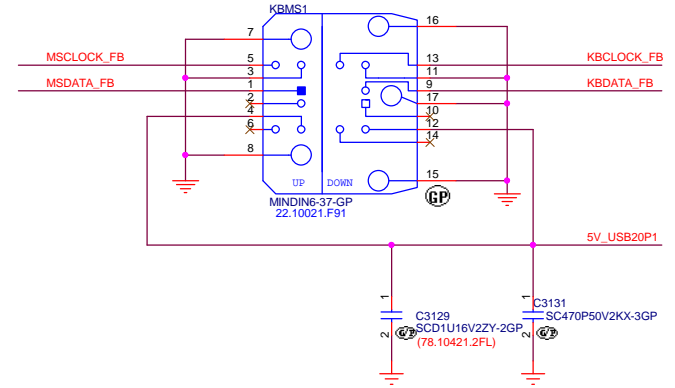
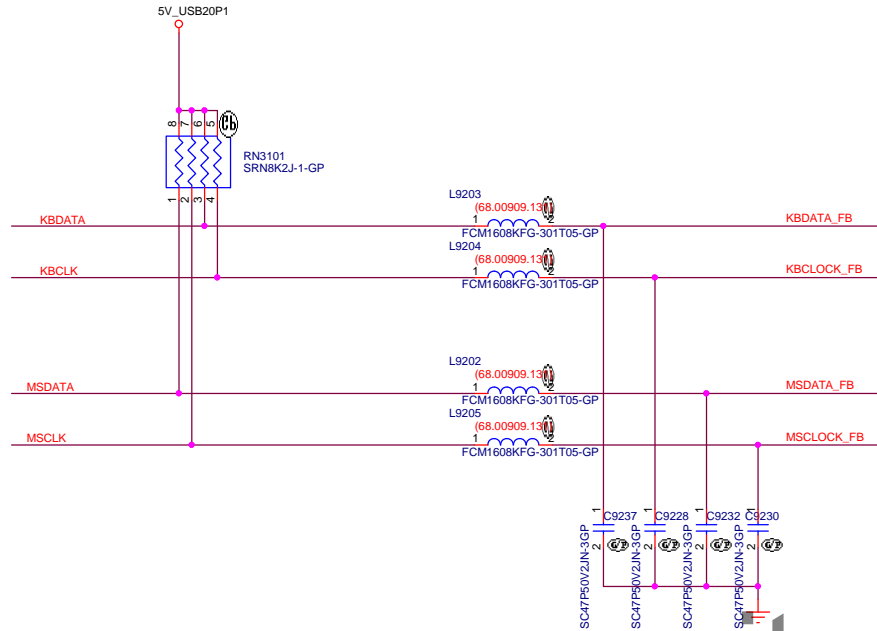
2015/4/16-1A Vita  
change TPMH1,R1157 F7 to (B,S\_)  
B: for B150 SKU  
S: for ECS Q170 SKU

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<Core Design>

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Title <b>TPM</b>		
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24 KBDATA  
24 KBCLK  
24 MSDATA  
24 MSCLK



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<b>PS2</b>			
Title	Document Number	Rev	
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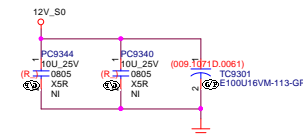
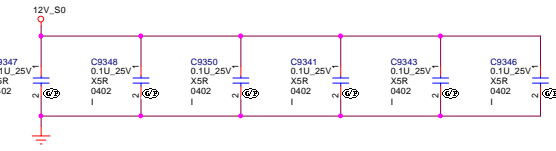
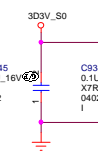
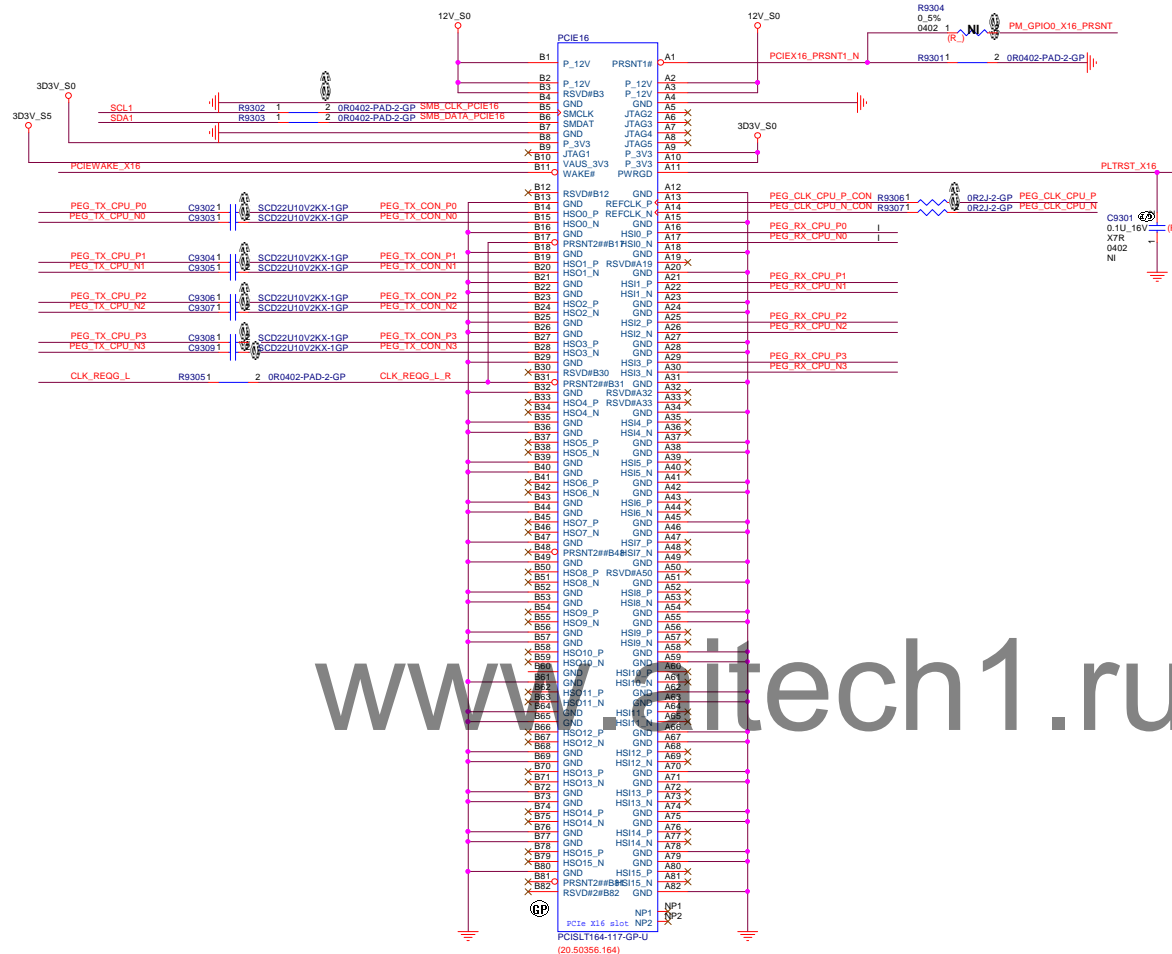
6.31.61.94 SCL1  
6.31.61.94 SDA1

7 PEG\_CLK\_CPU\_P  
7 PEG\_CLK\_CPU\_N  
6.18 PM\_GPIO0\_X16\_PRSNT

24 PLTRST\_X16

6 PCIEWAKE\_X16

6 CLK\_REQ0\_L

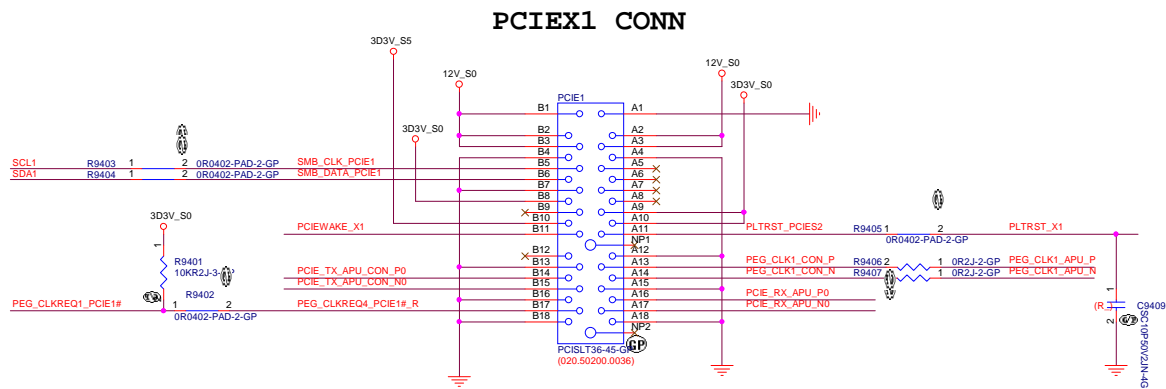


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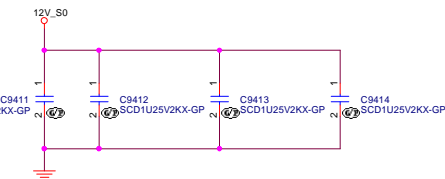
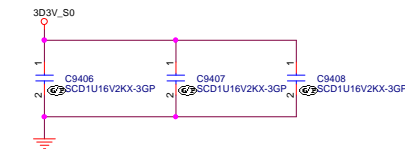
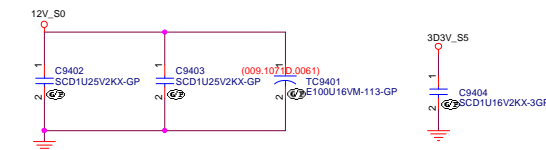
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		Hatchih, Taipei Hsien	
File	<b>Express Card:PCIE X16</b>		
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6,31,61,93 SCL1 >>>  
 6,31,61,93 SDA1 >>>  
 24 PLTRST\_X1 >>>  
 6 PCIEWAKE\_X1 <<<  
 3 PCIE\_TX\_APU\_CON\_P0 >>>  
 3 PCIE\_RX\_APU\_N0 >>>  
 3 PCIE\_RX\_APU\_P0 >>>  
 7 PEG\_CLK1\_APU\_P >>>  
 7 PEG\_CLK1\_APU\_N >>>  
 6 PEG\_CLKREQ1\_PCIE1# <<<




2014/11/26-SB Vita  
 del TC9401,TC9402 F7 P/N and reserve them



2014/12/24-SB Vita  
 change 12V cap to 25V tolerance

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Title			
<b>Smart Card PCIE X1</b>			
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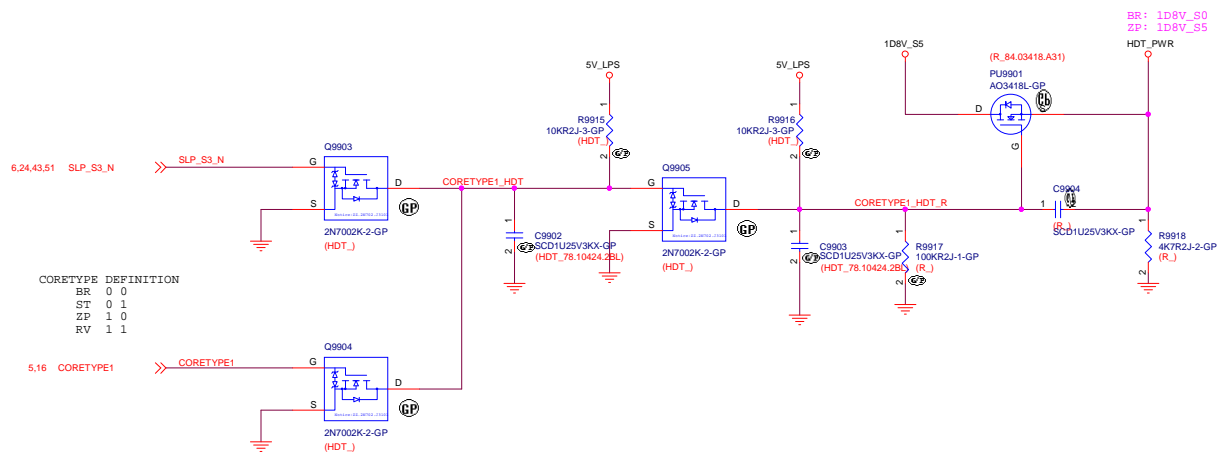
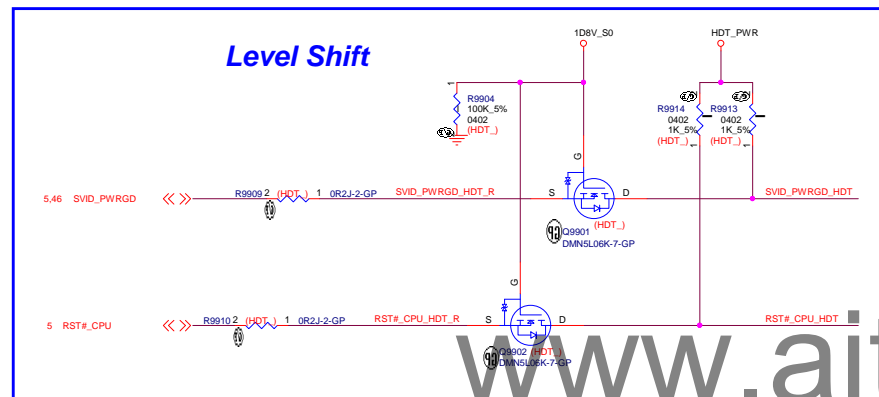
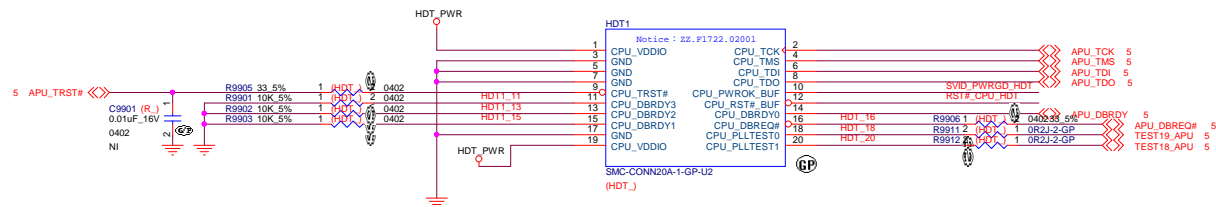
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## HDT Header



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Title			
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# APU GPIO

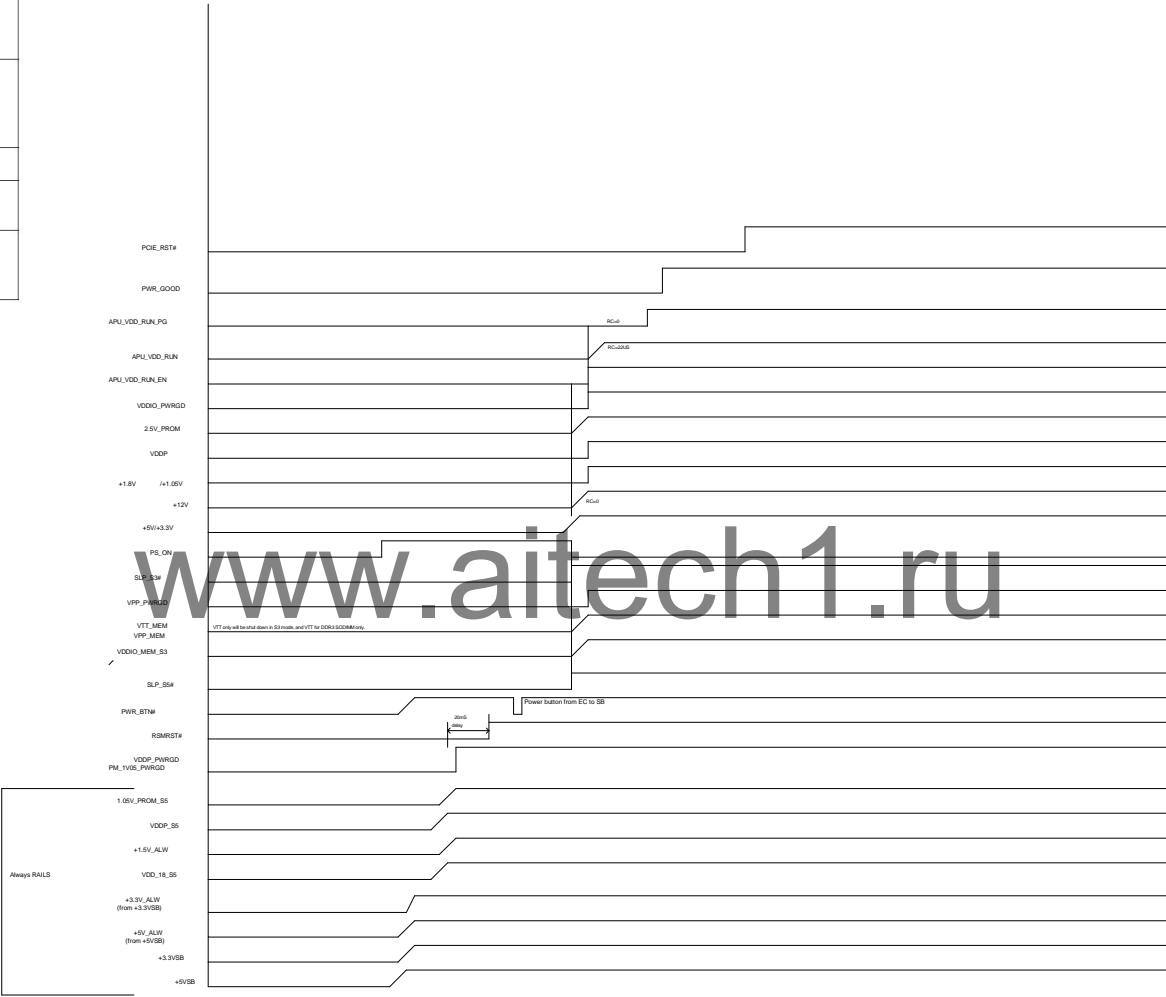
		Chipset Definition				I/OB7 GPIOs				Project Definition		ECIO Setting	
	Pin Number	Pin Name & Function		Type	Power/Viol	Pin Name		External Pull Up/Down					
UPC	14	SERRIO		DIOB	AI0C03	PLT_BSTR_APU	INT_SERRIO						
	15	LFPSIRAP		DIOB	AI0C03	LPC_FPSIRAP		PU 1k to 300V, 50					
	16	LAD0		DIOB	AI0C03	LAD0_SIG							
	17	LAD1		DIOB	AI0C03	LAD0_SIG		PU 1k to 300V, 50					
	18	LAD2		DIOB	AI0C03	LAD0_SIG							
	19	LAD3		DIOB	AI0C03	LAD0_SIG							
	20	PCOLDR		DIOB	AI0C03	LPC_CDR							
	21	PIEPB	GP44	DIOB	AI0C03	PC_PIEB_N		PU 4.7k to 300V, 50					
	43	CTVIA	GP31 FAN_TACS	InA	DIO_DIOB-DIOB	AI0C03	GP31		No Power For TACO3			Native	Output High
	62	IRPTA	GP12 FAN_CTLA	InA	DIO_DIOB	3I0B-AC03							
Serial Port 1	61	IRPTA	GP12 FAN_CTLA	InA	DIO_DIOB-DIOB	AI0C03	YK_HSTX_B		PU 1k to 300V, 50		Output High		
	68	DIRTA	GP13 JPA	DIOB	DIOB	AI0C03	JPA		PU 1k to 300V, 50		Output High		
	69	IRINT	GP41	InA	DIO_DIOB	AI0C03-3I0B	GP41		PU 1k to 300V, 50		Output High		
	80	SCUT1		DIOB	DIOB	AI0C03	SCUT1		PU 1k to 300V, 50		Output High		
	87	DIRTA	GP4 PCH_OCA JPA	InA	DIO_DIOB-DIOB	AI0C03-3I0B-AC03	LPC_BI0-2I0A		PU 4.7k to 300V, 50		Output Low		
	92	VINVOCCORE_VIO		A	AI0C03		VM_VCCP_R	PU 1k to 1V, VCC0R_CPU					
	93	VINVOCCORE_VIO_VIO2		A	AI0C03		VM_VCCP_R	PU 1k to 102V, VCC0R_MEM					
	94	VIN_VIO2_VIO2		A	AI0C03		VM_VIO2	PU 1k to 12V, 50					
	48	VIM	VIO121 VIOB_SEN	A	AI0C03-AC03-3I0B		VM_VIM	PU 4.8K/6K/8.4K/14K to 300V, 50					
	49	VIO		A	AI0C03-3I0B		VM_VIO	PU 10K/10K/15K to 5V, 50					
Infrared Sensor	49	VIOB		A	AI0C03-3I0B		VM_VIO	PU 10K/10K/15K to 5V, 50					
	46	VREF		AO	AI0C03		VM_VREF						
	46	TMFPA		AO	AI0C03		VM_TMFPND						
	44	TMFPA		AO	AI0C03		VM_TMFPND						
	38	COPEN		DIO	3I0B-3I0A		VM_COPEN	PU 1M to 300V, RTC_AUX					
	2	FAN_CTLB	GP1	InA	DIOB	AI0C03	GPU_FAN_CTLB_SIG	PU 2.2k to 300V, 50			Native		
	1	FAN_TACS	GP12	DIOB	DIO_DIOB	AI0C03	GPU_FAN_TACS_SIG				Native		
	1	FAN_CTLA	GP13	DIOB	DIO_DIOB	AI0C03	GPU_FAN_CTLA_SIG	PU 2.2k to 300V, 50			Native		
	3	FAN_TACS	GP17 MDAT	24V+	DIO_DIOB-DIOB	AI0C03-3I0B	MDAT	PU 1k to 300V, 50			Native		
	44	FAN_CTLA	GP13 MDAT	24V+	DIOB-DIOB-DIOB	AI0C03-3I0B	MDAT	PU 1k to 300V, 50			Native		
Keyboard Controller	3	KSTRT	GP12 MDAT	InA	DIO_DIOB	AI0C03	GP12	No Power For TP1K21			Output High		
	21	SD2		DIOB	AI0C03		GAT2A2	No Power For TP2149					
	22	BIASSTRT	GP15	DIOB	AI0C03		BIASSTRT	PU 1k to 300V, 50			Native		
	33	SVIS_VIOB		A	3I0B		SVIS_VIOB	PU 100 to 300V, 50					
	34	PANTRYIN		DIOB	3I0B		PANTRYIN	10k to 3V, LP1					
	34	PANTRYIN		DIOB	3I0B		PANTRYIN	PU 1k to 300V, 50					
	34	BUSSM		DIOB	3I0B		BUSSM	PU 1k to 300V, 50					
	34	BUSSM	GP13	InA	DIO_DIOB	AI0C03	BUSSM	PU 4.7k to 300V, 50			Native		
	2	PHWRIOB	GPU_VIO	DIOB	DIOB-DIOB-DIOB	AI0C03-AC03-3I0B	NC				Output High		
	2	PHWRIOB	GPU_VIO	DIOB	DIOB-DIOB-DIOB	AI0C03-3I0B-3I0B	NC				Output High		
PCIO SET	7	DPWRIOB	GP23	InA	DIOB-DIOB	3I0B	GP23-SUP	No Power For TP1K21			Output High		
	1	BIASSTRT	GP15	DIOB	DIOB	AI0C03							
	18	VIOB2EN	GP2 PCH_OCB SUBVARM	DIOB	DIOB-DIOB-DIOB-DIOB	AI0C03-3I0B-AC03-3I0B	NC						
	18	VIOB2EN	GP2 PCH_OCB SUBVARM	DIOB	DIOB-DIOB-DIOB-DIOB	AI0C03-3I0B-AC03-3I0B	NC						
	6	ATKPO	GP10	DIOB	DIOB	3I0B	PCH_IRST_APU_L	PU 1k to 300V, 50			Native		
	2	PHWRIOB	GPU_VIO	DIOB	DIOB-DIOB-DIOB	AI0C03-AC03-3I0B	NC						
	2	PHWRIOB	GPU_VIO	DIOB	DIOB-DIOB-DIOB	AI0C03-3I0B-3I0B	NC						
	7	DPWRIOB	GP23	InA	DIOB-DIOB	3I0B	GP23-SUP	No Power For TP1K21			Output High		
	1	BIASSTRT	GP15	DIOB	DIOB	AI0C03							
	18	VIOB2EN	GP2 PCH_OCB SUBVARM	DIOB	DIOB-DIOB-DIOB-DIOB	AI0C03-3I0B-AC03-3I0B	NC						
PCIO SET	6	PCIRSTRT	(C)RSTRT	GP10	DIOB	DIOB	PCH_IRST_APU_L	PU 1k to 300V, 50			Native		
	2	EST	ANSTGTS-D	GP12	GP43	24V+	8P-DIOB-DIOB-DIOB-DIOB	AI0C03-AC03-AC03-3I0B	SAKET_DATA	PU 2.2k to 300V, 50			
	2	ANSTGTS	ANSTGTS-C	GP4			DIOB-DIOB-DIOB-DIOB	AI0C03-AC03-3I0B	SAKET_DATA	PU 2.2k to 300V, 50			
	15	PCH_OCA	PCHIRSTRT	GP12	DIOB	DIOB-DIOB-DIOB-DIOB	AI0C03	NC_PCHIRSTRT			Native		
	5	PCH_OCB	GP22	DIOB	DIOB-DIOB	AI0C03-3I0B	CLIP_EMC_ENABLE	PU 1k to 300V, 50			Output High		
	5	PCH_OCB	GP22	DIOB	DIOB-DIOB	AI0C03-3I0B	CLIP_EMC_ENABLE	PU 1k to 300V, 50			Output High		
	5	PCH_OCB	GP22	DIOB	DIOB-DIOB	AI0C03-3I0B	CLIP_EMC_ENABLE	PU 1k to 300V, 50			Output High		
	5	PCH_OCB	GP22	DIOB	DIOB-DIOB	AI0C03-3I0B	CLIP_EMC_ENABLE	PU 1k to 300V, 50			Output High		
	5	PCH_OCB	GP22	DIOB	DIOB-DIOB	AI0C03-3I0B	CLIP_EMC_ENABLE	PU 1k to 300V, 50			Output High		
	5	PCH_OCB	GP22	DIOB	DIOB-DIOB	AI0C03-3I0B	CLIP_EMC_ENABLE	PU 1k to 300V, 50			Output High		
Power/GPIO	12	VIOB		DIOB	AI0C03		LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	14	ONDRST	GP1	DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		
	23	GP10D_JP1		DIOB	DIOB	AI0C03	LED_VIOB2EN	PU 1k to 300V, 50			Output High		

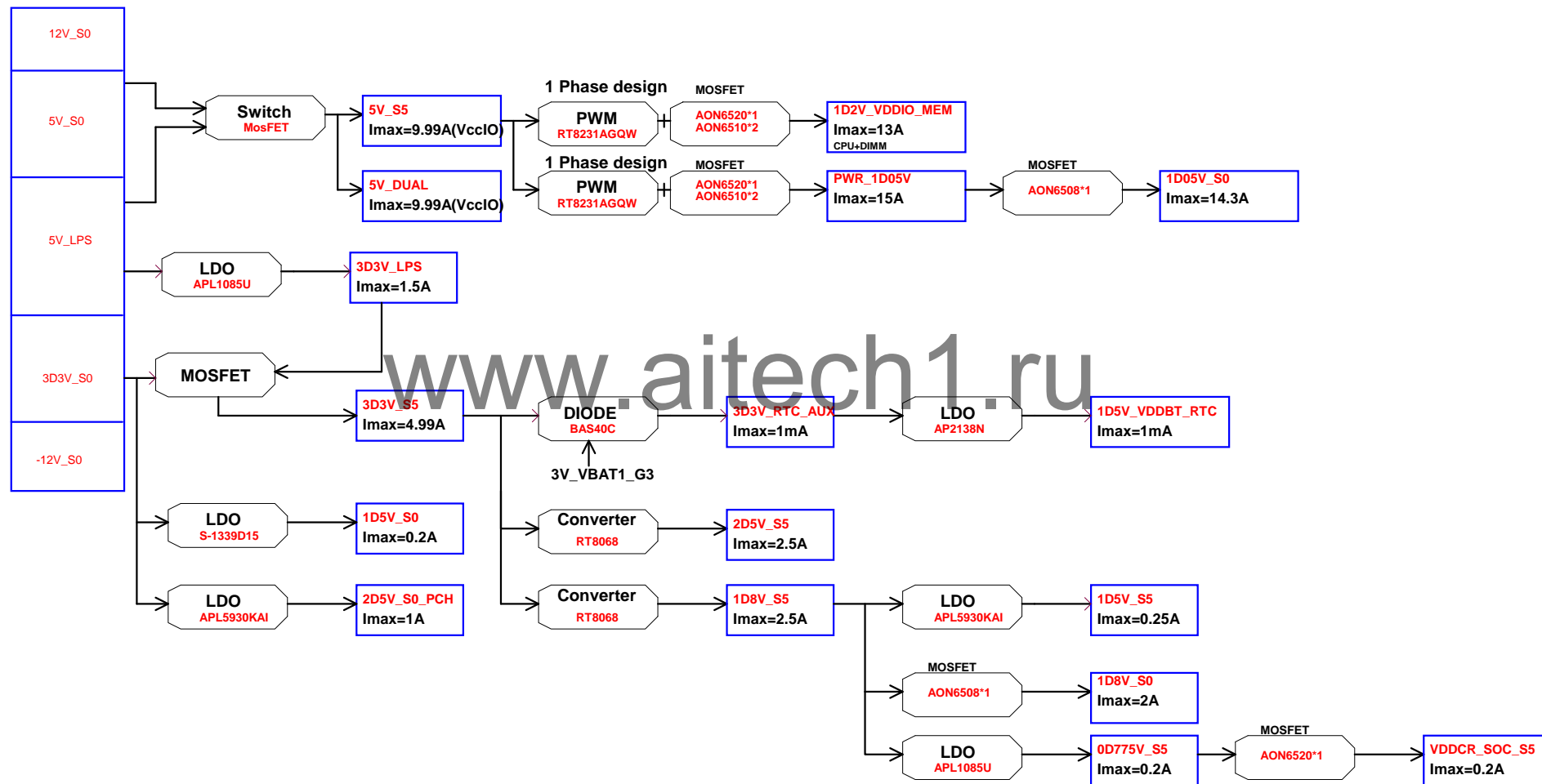
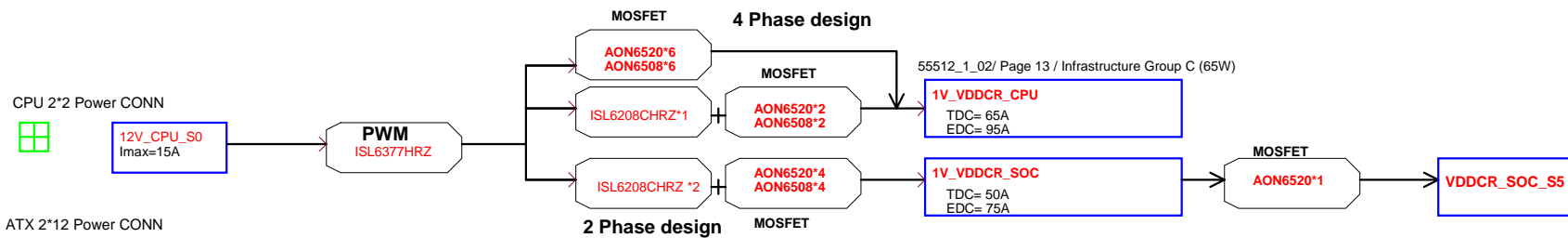
FCH chipset definition					AMD Bristol Ridge GPIO Table				
Pin Name	Description	Type	Power Well	Default	Internal Pull Up/Down	Pin Name	External Pull Up/Down	Type	
GPIO0	PWR_BTN_L	AGP00	IO	SS	Native	PULL-UP	PWR_PVRBTN	Pu 10K to 30V_S5	Native
GPIO1	SYS_RESET_L	AGP01	IO	SS	Native	PULL-UP	FP_RST_SW	Pu 10K to 30V_S5	Native
GPIO2	WAKE_L	AGP02	IO	SS	Native	PULL-UP	PCIE_WAKE	Pu 10K to 30V_S5	Native
GPIO3	AGP03		IO	SS	GR	PULL-UP	MOD5_SW_DET#	Pu 10K to 30V_S5	Input
GPIO4	AGP04		IO	SS	GR	PULL-UP	VR_DISABLE_L	Pu 10K to 30V_S5	Output High
GPIO5	AGP05	DEVSLP0	IO	SS	GR		IC	Pu 10K to 30V_S5	Output High
GPIO6	AGP06		IO	SS	GR	PULL-DOWN	FDT_OVRD_GPIO	Pu 10K to 30V_S5	Input
GPIO7	AGP08		IO	SS	GR	PULL-DOWN	IC		Input
GPIO8	AGP09	SOP00_DATAOUT	IO	SS	Native	PULL-UP	VR_DISABLE_N	Pu 10K to 30V_S5	Output High
GPIO9	SDA3	SOP00_SOP00_CLK	IO	SS	Native		LA0_DISABLE_L	Pu 2.2K to 30V_S5	Output High
GPIO11	AGP011	BLNK	IO	SS	GR	PULL-UP			Output High
GPIO16	USB_O0C_L	AGP016	IO	SS	Native	PULL-UP	USB00_OC_R#4	Pu 10K15K to 5V_DUAL	Native
GPIO17	USB_O0C_L	TD0AGP017	IO	SS	Native	PULL-UP	USB00_OC_R#4	Pu 10K15K to 5V_DUAL	Native
GPIO18	USB_O0C_L	TD0AGP018	IO	SS	Native	PULL-UP	USB00_OC_R#2#	Pu 10K15K to 5V_DUAL	Native
GPIO19	SC_L1	CC2_S0A0GP019	IO	SS	Native	PULL-UP	SC_L1	Pu 2K to 30V_S5	Native
GPIO20	SDA1	CC2_S0A0GP020	IO	SS	Native	PULL-UP	SCB_G0A	Pu 2.2K to 30V_S5	Native
GPIO21	LPC_PD_L	AGP021	IO	SS	Native		LPC_PD	No Power Rat T7701	Output High
GPIO22	LPC_PME_L	AGP022	IO	SS	Native	PULL-UP	SIO_PME_N	Pu 4.7K to 30V_S5	Native
GPIO23	AGP023	SOP00_LOAD	IO	SS	GR	PULL-UP	AGP023	No Power Rat T7601	Output High
GPIO24	USB_O0C_L	TD0AGP024	IO	SS	Native	PULL-UP	USB00_OC_F#4	Pu 10K15K to 5V_DUAL	Native
GPIO26	PCR_RST_L	EGP026	IO	SS	Native		PCR_RSTA_CPU	Pu 10K to 30V_S5	Native
GPIO40	AGP040	SOP00_DATAIN	IO	SS	GR	PULL-UP	IC		Native
GPIO42	SS_MUX_CTRL	EGP042	IO	SS	Native		SS_MUX_APU	Pu 100K to 30V_LPS	Output High
GPIO74	AGP074	IO	SS	GR	PULL-DOWN	SW_CMOS	P 0.2K to GND	Input	
GPIO74	LPCC09	EGP074	IO	SS	GR		STRAP_LPC_CLK_CPU_P0	Pu 2K to GND	Native
GPIO75	LPCC01	EGP075	IO	SS	Native		STRAP_LPC_CLK_CPU_P1	Pu 10K to 30V_S0	Native
GPIO76	AGP076	SPI_TPL_CS_L	IO	SS	Native		USB_GPO_C42	Pu 10K to 30V_S0	Input
GPIO76	FAIN04	AGP074	IO	SS	GR		USB_GPO_C13	Pu 10K to 30V_S0	Native
GPIO85	AGP085	FAIN079	IO	SS	GR	PULL-UP	FP_AD0_PRESENCE_N	Pu 10K to 30V_S5	Input
GPIO86	AGP086		Input	SS	GR	PULL-UP	LPC_SML_L	Pu 10K to 30V_S0	Output High
GPIO87	SER0Q	AGP087	IO	SS	Native	PULL-UP	INT_SERIRQ		Native
GPIO88	LPC_CLKRUN_L	AGP088	IO	SS	Native		P5W_GPIO		Output High
GPIO89	GENIUT_L		IO	SS	Native	PULL-UP	BIFF		Output High
GPIO91	AGP091	SPN0	IO	SS	GR	PULL-DOWN	SPN0		Native
GPIO91	CLK_REG0_L	SATA_B0_L/SATA_ZP0_L/AGP092	IO	SS	Native		IC		Output High
GPIO96	EGP096		Output	SS	GR	PULL-DOWN	IC		Output High
GPIO96	EGP096		Output	SS	GR	PULL-DOWN	IC		Output High
GPIO97	EGP097		IO	SS	GR	PULL-DOWN	HW0_EGP097	P 0.1K to GND	Input
GPIO98	EGP098		IO	SS	GR	PULL-DOWN	HW0_EGP098	P 0.1K to GND	Input
GPIO99	EGP099		IO	SS	GR	PULL-DOWN	HW0_EGP099	P 0.1K to GND	Input
GPIO100	EGP100		IO	SS	GR	PULL-DOWN	HW0_EGP100	P 0.1K to GND	Input
GPIO104	LA03	EGP0104	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P0		Native
GPIO105	LA01	EGP0105	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P1		Native
GPIO106	LA02	EGP0106	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P2		Native
GPIO107	LA03	EGP0107	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P3		Native
GPIO108	ESR_ALERT_L	LD00_EGP0108	Input	SS	Native	PULL-DOWN	IC		Output High
GPIO109	LPFRAME_L	EGP0109	IO	SS	Native		LPC_FRAMES_S0	Pu 10K to 30V_S0	Native
GPIO110	SC_L5	CC2_S0A0GP110	IO	SS	Native	PULL-UP	SMB_CLK_MAIN	Pu 2.2K to 30V_S0	Native
GPIO111	SC_L6	CC2_S0A0GP111	IO	SS	Native	PULL-UP	SMB_DATA_MAIN	Pu 2.2K to 30V_S0	Native
GPIO114	CLK_REG0_L	AGP0115	IO	SS	Native	PULL-UP			Output High
GPIO116	CLK_REG0_L	AGP0116	IO	SS	Native	PULL-UP	IC		Output High
GPIO117	SPL_CLK	ESPL_CLK0GP0117	IO	SS	Native	PULL-DOWN	SPL_CLK		Output High
GPIO118	SPL_CS_L1	EGP0118	IO	SS	Native		SPL_CS_CPU	Pu 10K to PWR_SPL_ROM	Output High
GPIO119	SPL_CS_L2	ESPL_CS_L0GP0119	IO	SS	Native				Output High
GPIO120	SPI_DI	ESPL_DAT0GP0120	IO	SS	Native	PULL-DOWN	SPI_CS_CPU		Output High
GPIO121	SPI_DO	ESPL_DAT0GP0121	IO	SS	Native	PULL-DOWN	SPI_CS_CPU		Output High
GPIO122	EGP0122	SPL_WP_L0ESR_DAT2	IO	SS	GR	PULL-UP	SPL_WP_CPU	Pu 1K to PWR_SPL_ROM	Output High
GPIO129	ESPL_RESET_L	KBRST_L	IO	SS	Native	PULL-UP	ESPL_RESET_LKBRST_L	Pu 10K to 30V_S0	Output High
GPIO130	SATA_ACT_L	AGP0130	IO	SS	Native		IC		Output High
GPIO131	CLK_REG0_L	SATA_B1_L/SATA_ZP1_L/EGP0131	IO	SS	Native		IC		Output High
GPIO132	CLK_REG0_L	EGP0132	Input	SS	Native		IC		Output High
GPIO133	EGP0133	SPL_HOLD_L0ESR_DAT3	IO	SS	GR	PULL-UP	SPL_HOLD_CPU		Output High
GPIO105	LA01	EGP0105	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P1		Native
GPIO106	LA02	EGP0106	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P2		Native
GPIO107	LA03	EGP0107	IO	SS	Native	PULL-DOWN	LPC_AD_S0_P3		Native
GPIO108	ESR_ALERT_L	LD00_EGP0108	Input	SS	Native	PULL-DOWN	IC		Output High
GPIO109	LPFRAME_L	EGP0109	IO	SS	Native		LPC_FRAMES_S0	Pu 10K to 30V_S0	Native
GPIO113	SC_L1	CC2_S0A0GP113	IO	SS	Native	PULL-UP	SMB_CLK_MAIN	Pu 2.2K to 30V_S0	Native
GPIO114	SC_L6	CC2_S0A0GP114	IO	SS	Native	PULL-UP	SMB_DATA_MAIN	Pu 2.2K to 30V_S0	Native
GPIO115	CLK_REG0_L	AGP0115	IO	SS	Native	PULL-UP	IC		Output High
GPIO116	CLK_REG0_L	AGP0116	IO	SS	Native	PULL-UP	IC		Output High
GPIO117	SPL_CLK	ESPL_CLK0GP0117	IO	SS	Native	PULL-DOWN	SPL_CLK		Output High
GPIO118	SPL_CS_L1	EGP0118	IO	SS	Native		SPL_CS_CPU	Pu 10K to PWR_SPL_ROM	Output High
GPIO119	SPL_CS_L2	ESPL_CS_L0GP0119	IO	SS	Native				Output High
GPIO120	SPI_DI	ESPL_DAT0GP0120	IO	SS	Native	PULL-DOWN	SPI_CS_CPU		Output High
GPIO121	SPI_DO	ESPL_DAT0GP0121	IO	SS	Native	PULL-DOWN	SPI_CS_CPU		Output High
GPIO122	EGP0122	SPL_WP_L0ESR_DAT2	IO	SS	GR	PULL-UP	SPL_WP_CPU	Pu 1K to PWR_SPL_ROM	Output High
GPIO129	ESPL_RESET_L	KBRST_L	IO	SS	Native	PULL-UP	ESPL_RESET_LKBRST_L	Pu 10K to 30V_S0	Output High
GPIO130	SATA_ACT_L	AGP0130	IO	SS	Native		IC		Output High
GPIO131	CLK_REG0_L	SATA_B1_L/SATA_ZP1_L/EGP0131	IO	SS	Native		IC		Output High
GPIO132	CLK_REG0_L	EGP0132	Input	SS	Native		IC		Output High
GPIO133	EGP0133	SPL_HOLD_L0ESR_DAT3	IO	SS	GR	PULL-UP	SPL_HOLD_CPU		Output High

AMD 200 chipset definition						Project Definition		
Pin Name	Description	Type	Power Well	Default	Internal Pull Up/Down	Pin Name	External Pull Up/Down	Type
GPI00		IO	VCC33	Native	PULLUP	FCPU_GPI05_X16_PRSNT	PULLUP	Input
GPI01		IO	VCC33	Native	PULLUP	FCPU_GPI085_PCIEX16_DET0	PULLUP	Input
GPI02		IO	VCC33	Native	PULLUP	FCPU_GPI088_PCIEX16_DET1	PULLUP	Input
GPI03		IO	VCC33	Native	PULLUP	FCPU_GPI090_PCIEX16_DET2	PULLUP	Input

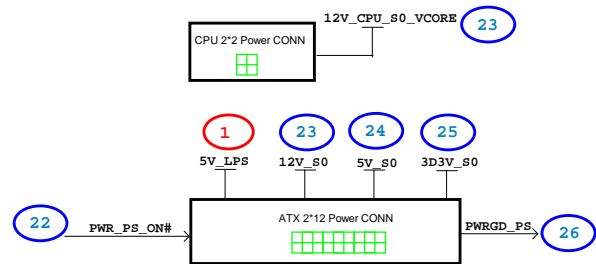
**Table 61. AM4 Power Sequencing Group Definitions with coin cell battery**

Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_SOC_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_SOC, VDDCR_CPU,

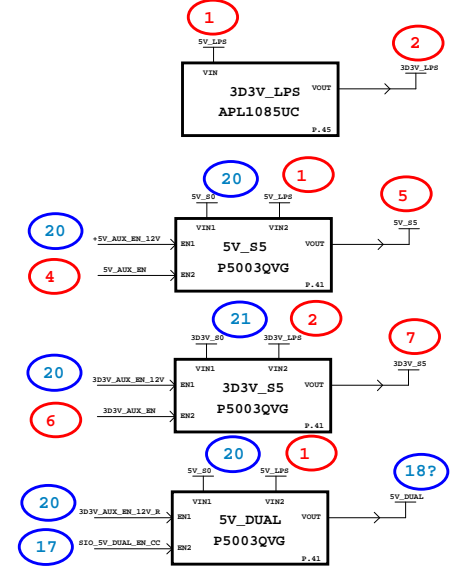




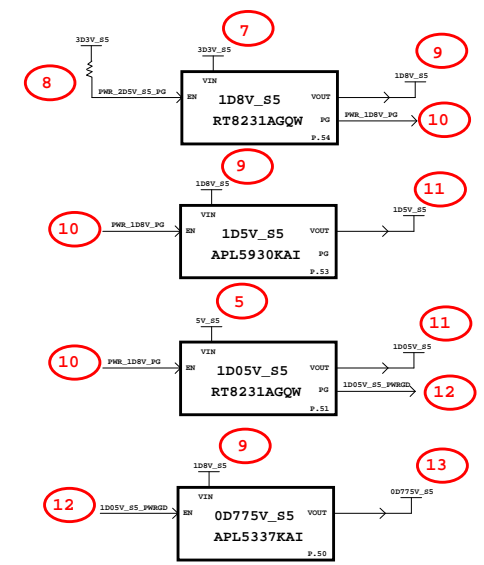
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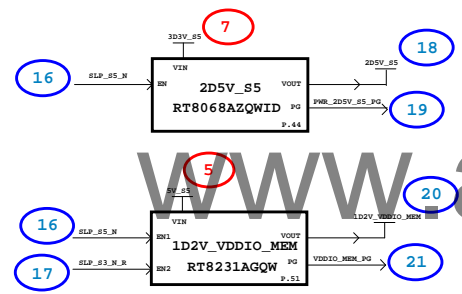
## Standby Power



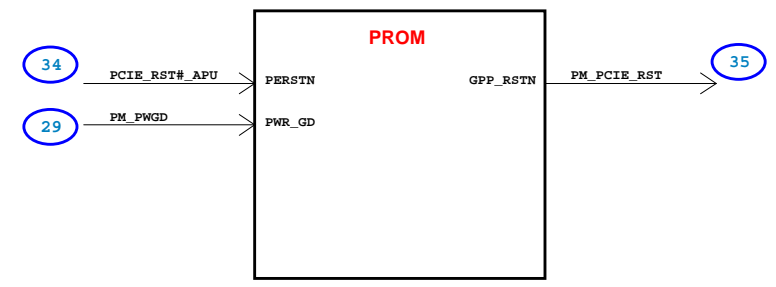
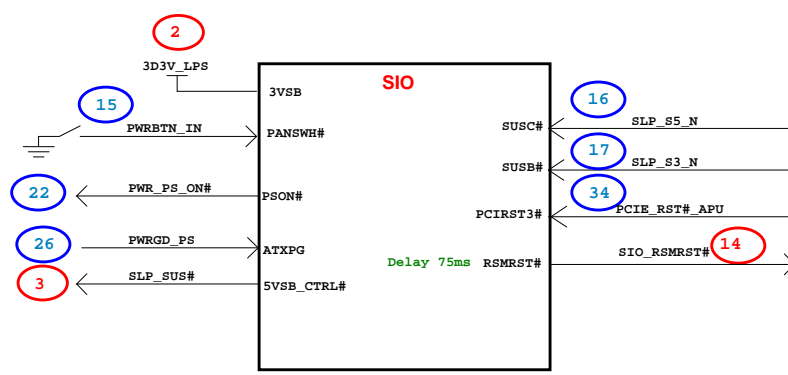
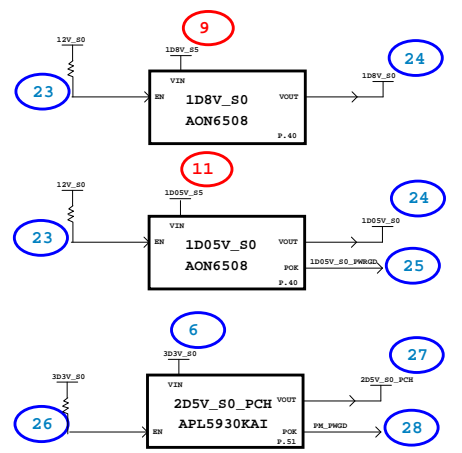
## Platform S5\_Rail



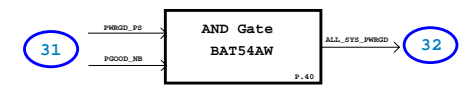
## Memory voltage



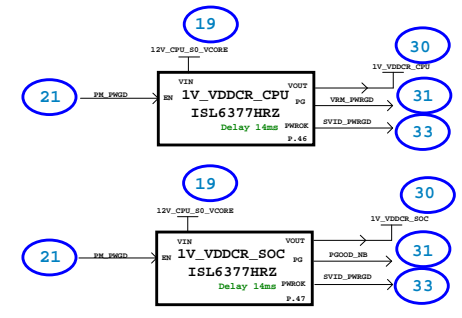
## Platform S0\_Rail



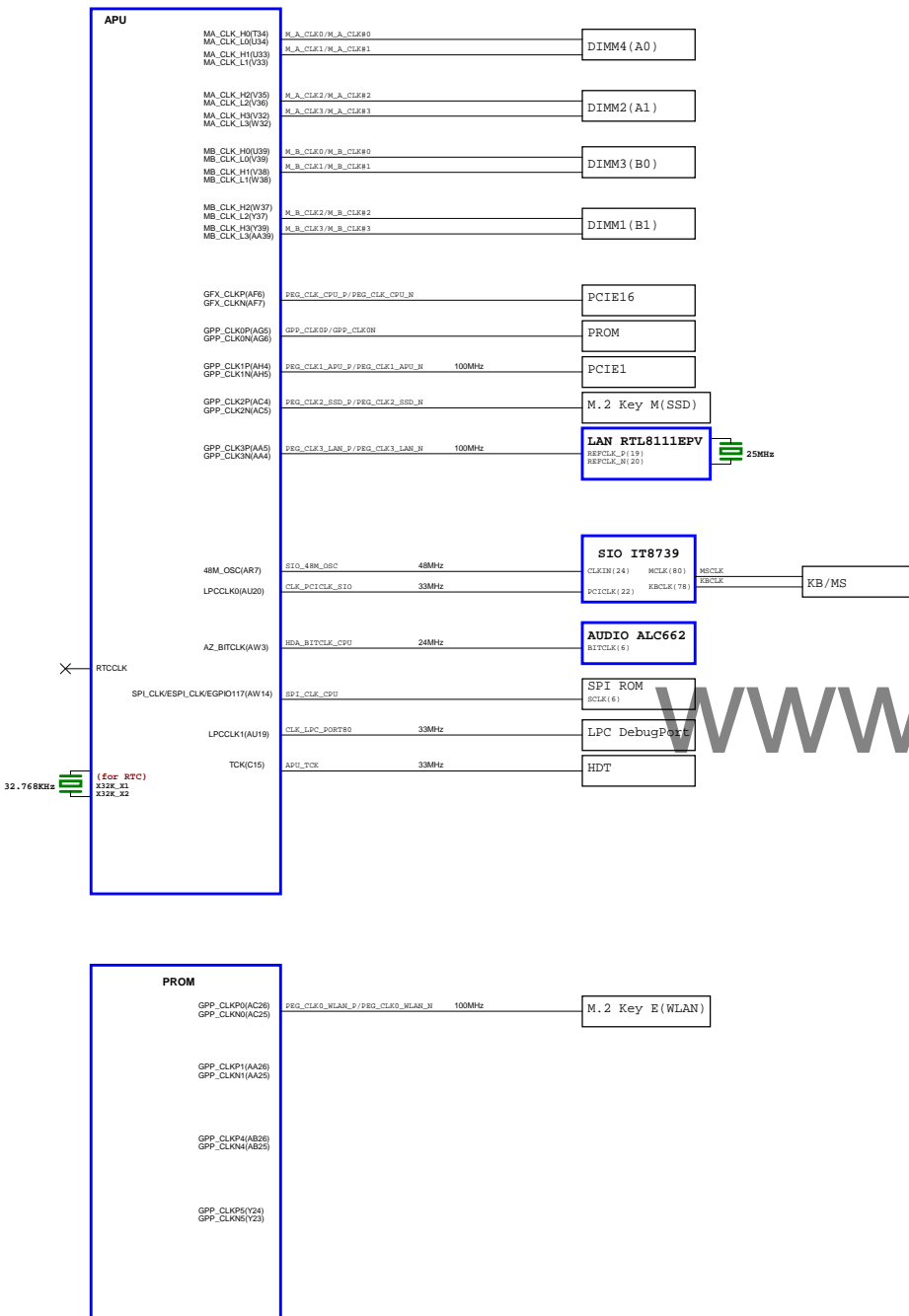
## AND Logic Gate



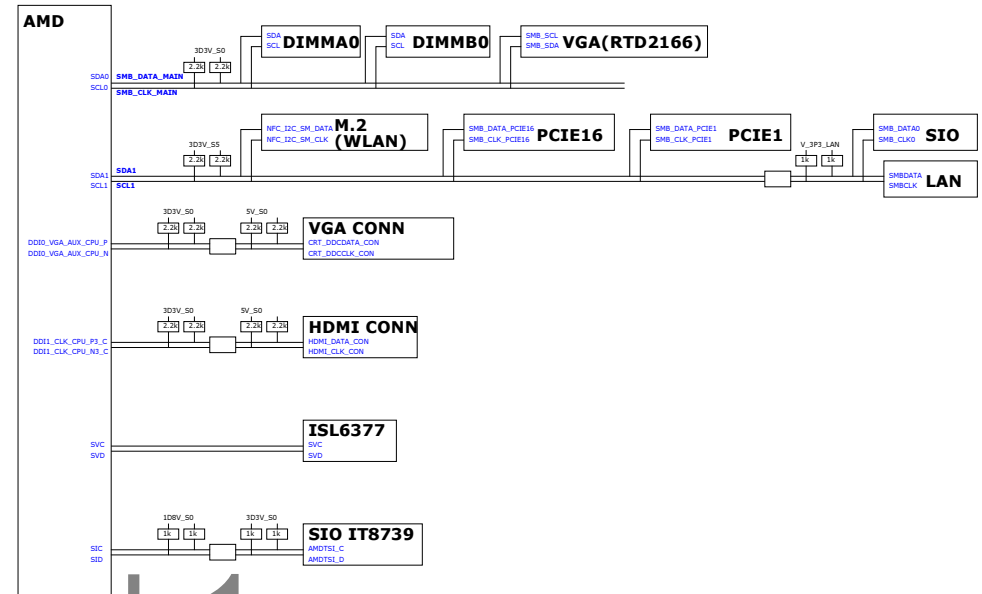
## CPU\_VCORE



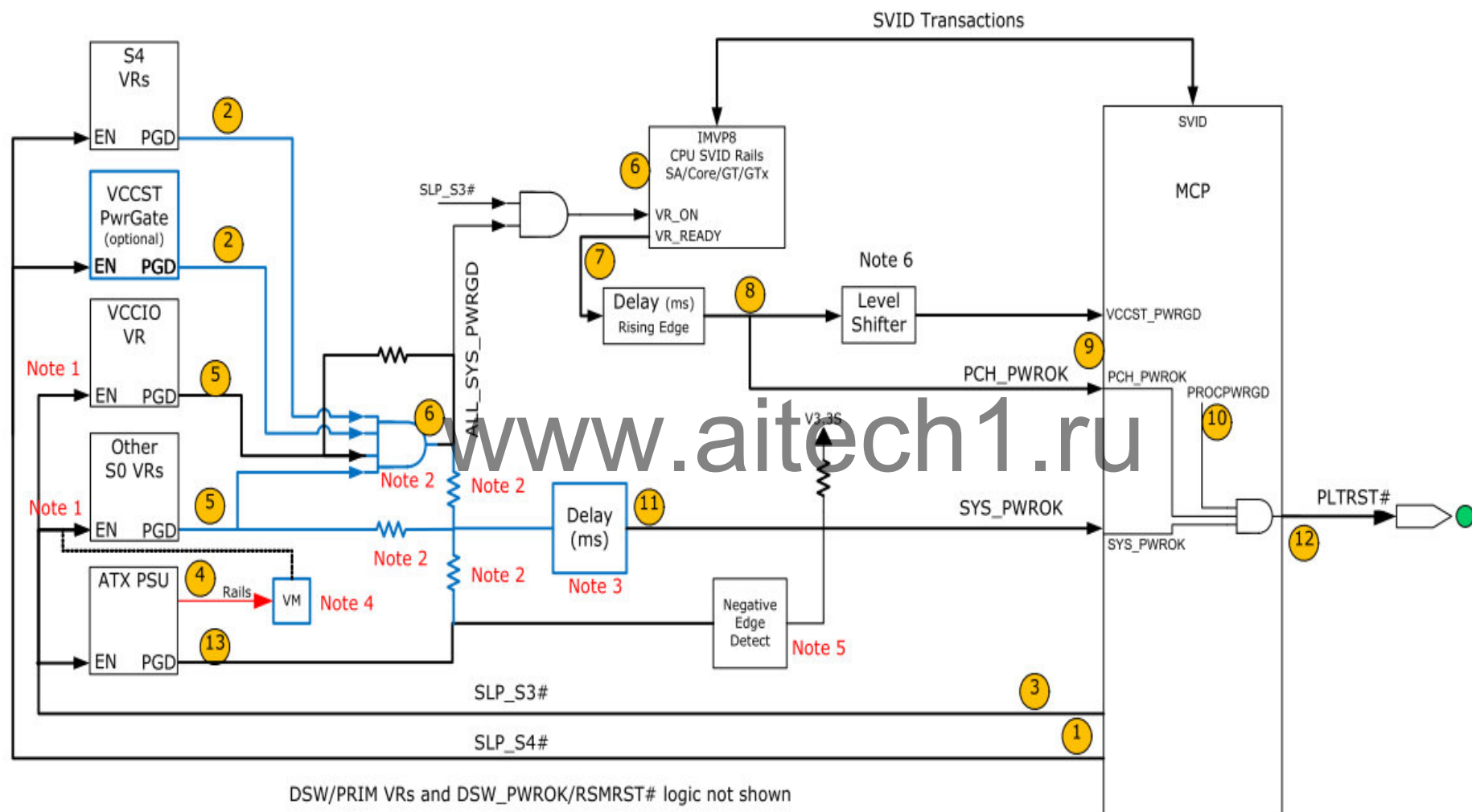
CLOCK BLOCK



## SMBUS BLOCK







# Wolverine Mother Board Schematics Revision History

Phase	DATE	Item	Page	Change List & Description
		1		
		2		
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